Reg No.:	00000CS40712190Yame:
110811011	00000C540/121/91

Seventh semester B.Tech examinations (S), September 2020

## **Course Code: CS407**

## **Course Name: DISTRIBUTED COMPUTING**

Max. M	Marks: 100 Duration:	3 Hours
	PART A	
	Answer all questions, each carries 4 marks.	Marks
1	In what all aspects distributed systems are better than centralized systems? Give	(4)
	examples of two applications for which distributed systems will be more	
	suitable.	
2	What are the different communicating entities in a distributed system?	(4)
3	Distinguish between synchronous and asynchronous distributed systems.	(4)
4	Describe the architecture of Skype overlay network.	(4)
5	Explain the characteristics of multicasting.	(4)
6	What is the role of Vice and Venus in AFS?	(4)
7	Does ring based mutual exclusion algorithm satisfy the happened before	(4)
	ordering criteria? Illustrate with an example.	
8	What are the criteria for evaluating the performance of a mutual exclusion	(4)
	algorithm?	
9	Explain the basic time stamp ordering rule.	(4)
10	Distinguish between forward and backward validation.	(4)
	PART B	
11	Answer any two full questions, each carries 9 marks.	(2)
11 a)	Explain processor pool model with diagram.	(3)
b)	Discuss the challenges in designing a distributed system.	(6)
12 a)	Illustrate the security model for distributed systems.	(6)
b)	Identify the failure category in the following events and define it:	(3)
	i.Dropped messages	
	ii.Corrupt/duplicate data	
	iii.Delayed transmission	
13 a)	Explain with an example the distributed service as a utility.	(4)
b)	How can processes and their interactions be secured in a distributed system?	(5)

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## PART C

14	a)	Answer any two full questions, each carries 9 marks.  Explain the request –reply protocol used in client server communication	(5)
	b)	Discuss IP multicast communication.	(4)
15	a)	What are the different call semantics in RPC?	(4)
	b)	Differentiate between NFS and AFS.	(5)
16	a)	Discuss the caching mechanisms in NFS.	(4)
	b)	Differentiate non- recursive and recursive navigation used in name service.	(5)
17	a)	PART D  Answer any two full questions, each carries 12 marks.  How the optimistic concurrency control to the serialization of transactions avoids	(6)
	b)	drawbacks of locking.  Explain the use of locks in two phase locking and strict two phase locking.	(6)
18	a)	Describe the working of bully algorithm with an example.	(6)
	b)	What is a nested transaction?	(6)
		Consider the following 'transfer' transactions T and U	
		<i>T</i> : a.withdraw(100); b.deposit(100);	
		U: c.withdraw(200); b.deposit(200);	
		Suppose that they are structured as pairs of nested transactions:	
		T1: a.withdraw(4); T2: b.deposit(4);	
		U1: c.withdraw(3); U2: b.deposit(3);	
		Compare the number of serially equivalent interleavings of T1, T2, U1 and U2	
		with the number of serially equivalent interleavings of $T$ and $U$ .	
19		Explain Ricart and Agrawala's algorithm for mutual exclusion. Discuss the	(12)
		performance of the algorithm. Explain the working of the algorithm in a	
		scenario of 4 processes P1, P2, P3 and P4 with P2 and P3 requesting to enter	
		into critical section with timestamps 28 and 36 respectively.	

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SEVENTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

## Course Code: CS401 Course Name: COMPUTER GRAPHICS

Max. Marks: 100 Duration: 3 Hours

#### **PART A** Marks Answer all questions, each carries 4 marks. 1 What do you understand by the aspect ratio and resolution of a display **(4)** screen in a raster scan display? 2 Write the flood fill algorithm for filling a polygon. **(4)** 3 Write the methods used to plot a dashed line segment. **(4)** 4 Given a triangle A(20,10) B(80,20) C(50,70). Find the co-ordinates of (4) vertices after each of the following transformation. (a) Reflection about the line x=y. (b) Rotation of the triangle ABC about vertex A in clockwise direction for an angle 90 degree. 5 Write the different tables used for representing polygon surfaces. Illustrate **(4)** with an example. Describe the techniques that can be used to provide text clipping in a 6 **(4)** graphics package. 7 Explain about different types of parallel projections. **(4)** 8 What do you understand by correlation and convolution operations in case of **(4)** image processing? 9 Write the Z-buffer algorithm for hidden surface removal. **(4)** 10 What do you understand by the following terms with respet to pixels. (4) Neighbours, Adjacency, Connectivity. PART B Answer any two full questions, each carries 9 marks. 11 Explain the working of a random scan display system with suitable diagram. (6) a) b) Explain the working of a beam penetration CRT. (3) 12 Write the midpoint circle drawing algorithm. **(4)** a) Use midpoint circle drawing algorithm to plot a circle whose radius =20 b) (5) units and center is (50, 30). 13 A mouse is picked up and placed in another position. Whether the position of a) (2) the mouse pointer change. Justify your answer. Explain the working of a light pen. b) (3)

**(4)** 

Write the scan line algorithm for filling a polygon.

c)

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		PART C	
		Answer any two full questions, each carries 9 marks.	
14	a)	Given a clipping window A(-20,-20), B(40,-20), C(40,30) and D(-20,30). Using Cohen Sutherland line clipping algorithm, find the visible portion of the line segment joining the points P(-30,20) and Q(60,-10).	(6)
	b)	Derive an equation for window to viewport transformation by specifying the sequence of basic transformations involved.	(3)
15	a)	What are the steps for general 3D rotation if the rotation axis is not parallel to any one of the principal axis. The rotation axis is defined by the points $P1(x1,y1,z1)$ and $P2(x2,y2,z2)$ . Write down the composite matrix representation.	(9)
16	a)	Explain Sutherland Hodgeman polygon clipping algorithm with illustrations.	(5)
	b)	Describe the transformation which reflects a 2-D object about a line L which has a y-intercept(0,b) and an angle of intersection theta degree w.r.t. to the x-axis.	(4)
		PART D	
		Answer any two full questions, each carries 12 marks.	
17	a)	Explain in detail the scan line algorithm for visible surface detection by pointing out the data structures used in this algorithm.	(7)
	b)	How the cyclic overlaps of surfaces are eliminated in scan line algorithm?	(2)
	c)	In case of an A-buffer algorithm, what information is stored in a linked list.	(3)
18	a)	Explain the fundamental steps in Digital Image Processing with a neat diagram?	(8)
	b)	The gray levels in an image $g1(x,y)$ range from <b>a</b> to <b>b</b> . It is decided to change it into an image $g2(x,y)$ in which the gray levels range from <b>c</b> to <b>d</b> using a linear transformation of its gray levels. Derive the equation for $g2(x,y)$ as a function of $g1(x,y)$ by specifying the steps.	(4)
19	a)	Explain the Robert's, Prewitt's and Sobel's edge detectors.	(6)
	b)	Derive the transformation matrix for perspective projection with the	(6)

to be at the viewing co-ordinate origin.

projection reference point at position Z<sub>prp</sub> along the Z<sub>v</sub> axis and the view plane at Z<sub>vp</sub>. Write the perspective transformation equations (i) if the view place is taken to be the uv plane (ii) if the projection reference point is taken

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SEVENTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

## Course Code: CS401 Course Name: COMPUTER GRAPHICS

Max. l	Max. Marks: 100 Duration: 3 H	
	PART A  Answer all questions, each carries 4 marks.	Marks
1	Suppose you have a raster system designed using an 8 inches $\times$ 10 inches screen	(4)
	with a resolution of 100 pixels per inch in each direction. What frame buffer size	
	is required if 6 bits are stored per pixel in the buffer?	
2	Write the midpoint circle drawing algorithm.	(4)
3	a) List the advantages of using Bresenham's line drawing algorithm.	(2)
	b) What is the purpose of a frame buffer in a display system?	(2)
4	How does Cohen Sutherland algorithm determine whether a line is visible,	(4)
	invisible or a candidate for clipping based on the region codes assigned to the	
	end points of the line?	
5	A triangle ABC with coordinates A(0,0), B(6,5), C(6,0) is scaled with scaling	(4)
	factors Sx=2 and Sy=3 about the vertex C(6,0). Find the transformed coordinate	
	points.	
6	Write the 3D translation matrix for moving an object by -2 units, -4 units and -6	(4)
	units respectively in x, y and z directions.	
7	Describe Histogram and also the type of information which obtained from a gray	(4)
	level histogram	
8	Briefly describe the various classification of the visible-surface detection	(4)
	algorithms.	
9	Is there any point at which a set of projected parallel lines appears to converge?	(4)
	Justify your answer.	
10	What is edge detection? Explain any one edge detection technique in digital	(4)
	image processing.	
	PART B	
	Answer any two full questions, each carries 9 marks.	

11 a) Describe in detail about emissive and non-emissive flat panel displays. (5)

	b)	Explain the working principle of a Refresh CRT monitor with suitable diagrams.	(4)
12	a)	Write the boundary fill algorithm for filling a polygon using eight connected	(4)
	1 \	approach.	( <b>5</b> )
	b)	Use mid-point circle drawing algorithm to plot a circle whose radius =20 units and centre at (50,30).	(5)
13	a)	Write a note on any two interactive graphics input devices.	(3)
	b)	Scan convert the line segment with end points (30,20) and (15,10) using DDA line	(4)
	٠,	drawing algorithm	(.)
	c)	What are the advantages and disadvantages of DDA line drawing algorithm	(2)
		PART C	
		Answer any two full questions, each carries 9 marks.	
14	a)	Perform a 45 degree rotation of a triangle ABC having the vertices at A(0,0)	(6)
		B(10,10) and C(50,20)	
		i. About the origin	
		ii. About an arbitrary point P(-10,-10)	
	b)	Describe the tables used to represent a polygon surface.	(3)
15	a)	Explain the window to viewport coordinate transformation and also derive the	(5)
		scaling factors during the transformation.	
	b)	Show that the composition of two rotation is additive by concatenating the	(4)
		matrix representation for $R(\Theta 1)$ and $R(\Theta 2)$	
16	a)	Show that transformation matrix for a reflection about the line y=x is equivalent	(4)
		to a reflection relative to the x axis followed by a counter clockwise rotation of	
		90 degree.	
	b)	Write Weiler - Atherton polygon clipping algorithm with suitable example.	(5)
		PART D	
		Answer any two full questions, each carries 12 marks.	
17	a)	Compare object space and image space method of visible surface detection	(3)
		technique.	
	b)	Describe in detail the depth buffer visible surface detection technique. Derive	(9)
		the equation to find the depth values for a surface position (x, y).	
18	a)	What is mean by convolution? Give applications of 2D convolution in the field	(4)
		of image processing.	
	b)	Distinguish between cavalier and cabinet projection.	(4)
	c)	Explain scan line algorithm with suitable example.	(4)

19 a) What is parallel projection? Describe orthographic and oblique parallel (6) projection in detail.

b) Consider the image segment shown below. (6)

3 1 2 <u>1</u> **(q)** 2 2 2 0 1 2 1 1 2  $(\mathbf{p}) \quad \underline{\mathbf{1}}$ 0 1

i) Compute the lengths of shortest 4, shortest 8 and shortest m paths between pixels p and q where  $V=\{0,1\}$ . If a particular path does not exist between these two points, explain why.

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### APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech S7 (S) Examination Sept 2020

## Course Code: CS401 Course Name: COMPUTER GRAPHICS

Max. Marks: 100 **Duration: 3 Hours PART A** Answer all questions, each carries 4 marks. Marks Describe simple random scan display system and draw its architecture. 1 (4) 2 Describe Flat Panel Display and explain its different categories. (4) 3 Which are the steps involved in window to viewport coordinate transformation (4) in 2D? 4 Magnify the triangle ABC with A(0, 0), B(1, 1) and C(5, 2) to twice its size (4) while keeping C(5, 2) fixed. 5 Show that the composition of two successive rotations are additive i.e.  $R(\Theta 1)$ . (4)  $R(\Theta 2) = R(\Theta 1 + \Theta 2).$ 6 Derive the linear equation for a 3D object and test whether the coordinates are (4) inside or outside the plane. 7 Define the terms (i) Centre of projection (ii) Principal vanishing point (4) 8 Differentiate between the object space and image space method for the hidden (4) surface removal of an image. 9 Describe the basic concepts of sampling and quantization with a neat sketch. (4) 10 Write any six differences between perspective projection and parallel projection (4) PART B Answer any two full questions, each carries 9 marks. Generate the points between the end points of a line viz.(2,2) and (9,6) by using 11 (5) Bresenham's line drawing algorithm. b) Scan convert the line segment with end points (30,20) and (15,10) using DDA (4) line drawing algorithm. 12 a) With a suitable figure, describe the shadow masking techniques in CRT. (5) b) Write a note on any two interactive graphics input devices. (4) 13 a) Derive the Initial decision parameter of midpoint circle drawing algorithm. (6) b) Describe the relevance and various methods of inside-outside test used in (3) polygon filling.

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### **PART C**

Answer any two full questions, each carries 9 marks.

- Explain the Sutherland Hodgeman algorithm for polygon clipping with an (9) example.
- 15 Consider a triangle at (2,2), (10,2), (2,10). Perform the following 2D (9) transformations in succession and find the resultant vertices
  - (i) Scale with respect to (2,2) by scaling factors (2,2) respectively along x and y directions.
  - (ii) Rotate by 90° counter clockwise direction
- 16 a) Briefly explain the steps involved in clipping a line using Mid point (5) Subdivision algorithm.
  - b) Explain how polygon meshes are used for 3D modelling. (4)

### **PART D**

Answer any two full questions, each carries 12 marks.

- 17 a) Differentiate between oblique and orthogonal projection. (4)
  - b) Explain histogram matching with an example. (8)
- 18 a) Describe in detail the depth buffer visible surface detection technique. Derive (9) the equation to find the depth values for a surface position (x, y).
  - b) Explain the terms adjacency and connectivity in the context of digital images. (3)
- 19 a) Explain the scan —line method used in visible surface detection with an example. (4)
  - b) Consider the image segment and compute the length of the shortest 4-, 8- and (8) m-path between p and q by considering two set of values for V:
    - $(i)V = \{0,1,2\}$

 $(ii)V = \{1,2\}$ .

If a particular path does not exist explain the reason for the above two cases of

**V** . 3 2 0 1 4 0 1 0 2(q)3 1 4 (q)3 0 4 2 1 3 1 2 0 4

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## SEVENTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

## Course Code: CS403 Course Name: PROGRAMMING PARADIGMS

Max. Marks: 100 Duration: 3 Hours

#### **PART A** Marks Answer all questions, each carries 4 marks. 1 Show what is side-effect in an expression with the help of an example? **(4)** 2 Can a user access a non-local object in case of subroutines, give valid reasons. **(4)** 3 With example, briefly explain structural and named equivalence. **(4)** 4 Describe the parameter modes used in ADA. **(4)** Consider the function (define double(lamda(x)(+xx))), Evaluate the expression 5 **(4)** (double(\*23)) in applicative order as well as normal order. With help of an example, show how exception is handled in C++? 6 (4) 7 Differentiate greedy and minimal matches. Generate greedy and minimal **(4)** matches for the pattern /(cd)+/ in the string acdcdcdcde 8 Explain constructors and destructors **(4)** 9 What is a thread pool in Java? What purpose does it serve? (4) 10 In what sense is fork/join more powerful than co-begin? **(4)** PART B Answer any two full questions, each carries 9 marks. 11 a) Write a pseudo code to find factorial of a number based on recursive and tail **(4)** recursive procedure. b) Give the code for the following source with and without short-circuit evaluation. (5) if $(A \le B)$ and $(C \le D)$ or (E! = F) then then clause else else clause Summarize the differences among mark and sweep, stop and copy, and 12 a) (5) generational garbage collection. b) How records are represented in programming languages? Explain. **(4)** 13 a) Consider the following pseudocode: **(4)** x : integer := 3y : integer := 4procedure add x := x + yprocedure second(P : procedure) x : integer := 5P() procedure first

y : integer := 6

		second(add) first() write integer(x) (a) What does this program print if the language uses static scoping? Give reasons	
		(b) What does it print if the language uses dynamic scoping and give reasons	
	b)	What are the memory layouts used in arrays? How the address calculation is	(5)
		done in three dimensional arrays?	
		PART C	
		Answer any two full questions, each carries 9 marks.	
14	a)	Explain co-routine? Why cactus-stack is used in co-routine?	(6)
	b)	In what sense do generics(template) serve a broader purpose in C++?	(3)
15	a)	Explain how to maintain the static link and dynamic link during a subroutine	(4)
		call.	
	b)	(let ((a 6) (b 8) (square (lambda (x) (* x x))) (plus +)) (sqrt (plus (square a) (square b))))	(5)
		Write the output of the above code? Explain how let and lambda construct works	
16	a)	Define lazy evaluation with an example.	(3)
	b)	How database manipulation is carried out in Prolog using assert and retract?	(3)
	c)	What are the unification rules used in Prolog?	(3)
		PART D  Answer any two full questions, each carries 12 marks.	
17	۵)		(0)
17	a) b)	Explain the innovative features of scripting languages.  Summarize the visibility rules used in C++.	(9) (3)
18	a)	Compare and differentiate the data types of popular scripting languages to those of compiled languages like C.	(6)
	b)	What is a semaphore? What operations does it support? How binary and general semaphore does differ?	(6)

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b) What is a JIT compiler? What are its potential advantages over (3)

19 a) Describe six different mechanisms(principles) commonly used to create new (9)

threads of control in a concurrent program

interpretation/conventional compilation?

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SEVENTH SEMESTER B.TECH DEGREE EXAMINATION(S), MAY 2019

## Course Code: CS403 Course Name: PROGRAMMING PARADIGMS

Max. Marks: 100 **Duration: 3 Hours** 

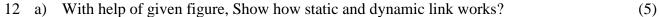
## PART A Marks Answer all questions, each carries 4 marks. 1 What is binding time? Explain the distinction between the lifetime of a name to object (4) binding and its visibility. 2 Does C have enumeration controlled loops? Explain. (4) 3 What is a dope vector? What purpose does it serve? (4) 4 What is a higher order function? Give three examples. (4) 5 What are facts, rules and queries? (4) How does an in-line subroutine differ from a macro? 6 (4) 7 Explain how reader writer lock differs from a normal lock. (4) 8 What is busy waiting? What is its principal alternative? (4) 9 Does a constructor allocate a space for an object? Explain. (4) What is a V-table? How is it used? 10 (4) **PART B** Answer any two full questions, each carries 9 marks. 11 a) From the given fragment of code, identify the scope of each names used in code and (6)also define closest nested scope rule. procedure P1(A1 : T1); var X : real; procedure P2(A2 : T2); procedure P3(A3 : T3); begin ... (\* body of P3 \*) end; begin ... (\* body of P2 \*)

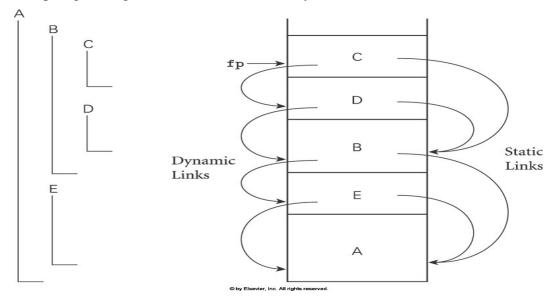
end;

procedure P4(A4 : T4);

```
function F1(A5 : T5) : T6;
var X : integer;
...
begin
... (* body of F1 *)
end;
...
begin
... (* body of P4 *)
end;
...
begin
... (* body of P1 *)
end;
```

b) C language is not a strongly typed language. Can you give the reason that prevents C (3) to be strongly typed language?





b) What is the difference between value model of variables and a reference model of variables? Why is the distinction important?

13 a)
Consider the following records of a particular language. Let the size of each char variable be 1 byte, int be 4 bytes and float be 8 bytes.

1) struct student

2) union student

{ { char name[2]; char name[2]; int age; int age; float mark; float mark; } } Draw the memory layout for the records (1) and (2) for a 32-bit aligned machine. b) Explain the difference among strict and loose name equivalence (3) PART C Answer any two full questions, each carries 9 marks. Describe four parametric-passing modes. How does a programmer choose a parameter 14 (6)mode in a particular scenario Describe three alternative means of allocating co-routine stacks. b) (3) 15 a) What is a subroutine calling sequence? What does it do? What is meant by subroutine (6)prologue and epilogue? b) How let and letrec constructs work in scheme? (3) 16 a) rainy(seattle). (6)rainy(rochester). cold(rochester). snowy(X) := rainy(X), cold(X).From the above facts and rules, explain the backtracking strategy in Prolog. b) Draw a DFA to accept all strings of zeros and ones containing an even number of (3) each. How a Scheme interpreter works in this case? PART D Answer any two full questions, each carries 12 marks. 17 Generate strings and output from the following pattern (9) /a(bc)?/ i) ii) /a(bc)+/ iii) /a(bc){3}/ iv) /a(bc){2,}/ /a(bc){1,3}/ v) /b[aeiou]d/ vi) vii) /0x[0-9a-fA-F]+/ viii) \$foo = "albatross"; foo = s/[aeiou]/-/g;\$foo = "albatross"; ix) \$foo = s/lbat/c/; b) Explain the difference between dynamic and static method binding (3)

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SEVENTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

## Course Code: CS403

### Course Name: PROGRAMMING PARADIGMS Max. Marks: 100 Duration: 3 Hours **PART A** Marks Answer all questions, each carries 4 marks. 1 What is Referencing Environment? Explain the difference between Deep and (4) Shallow binding of Referencing Environment? 2 What are holes? Why do they arise in records? What problems do they cause? (4) What can be done to reduce these problems? 3 What are variant records? Give a sample and its memory layout. (4) 4 Compare co-routine and subroutine? (4) 5 Distinguish the three access specifiers in C++. (4) 6 Differentiate Abstract classes and Concrete classes. (4) 7 What are the benefits of Java Virtual Machine? (4) 8 Define Horn clause and its components. (4) 9 Differentiate between co-routines and threads. (4) 10 What is RPC and stub compiler? (4) PART B Answer any two full questions, each carries 9 marks. 11 Name the seven categories of control flow mechanisms in various programming (7) languages. Explain each one with sample code. b) Define orthogonality as a language design tool (2) 12 a) Compare primitive and composite data types. (4) b) Explain static and dynamic type checking with example (5) 13 a) What is the problem of dangling references? How is it addressed in different (5) languages? b) What is short-circuit Boolean evaluation? Why is it useful? How it is (4) implemented?

## **PART C**

Answer any two full questions, each carries 9 marks.

14 a) (5) What are the purposes of stack pointer and frame pointer registers? Explain how

these pointers are associated with subroutine linkages.

- b) What is generic subroutine? Give the merits of using them in our programs? (4)
- 15 a) List and explain any three features of functional languages. (3)
  - b) Write the result of the Scheme expressions and explain how do you derived the result:
    - i) (let((a 33))
      let((a 32)
      (ba))
      (+ab)))
      ii) (let((x 24))
      (\* x
      (let((x (/ x 3)))
      (+xx))))
- 16 a) Explain the difference between facts, rules and queries. Give example for each one. (6)
  - b) What is in-line subroutine? How does it differ from macro? (3)

## **PART D**

Answer any two full questions, each carries 12 marks.

- 17 a) What is shared memory? What are the two types of synchronization issues they face? Explain how these issues can be solved?
  - b) Explain the three principal issues in using message passing. (6)
- 18 a) List and explain the object oriented programming concepts. (6)
  - b) What is shared inheritance? What is ambiguity problem in this and how the problem can be removed? (6)
- 19 a) What are constructors and destructors? Discuss the different forms of (6) constructors included in C++.
  - b) Explain the Busy-wait synchronization mechanism. (6)

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## APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech S5 (S) (PT) Exam Sept 2020

## **Course Code: CS403** Course Name: PROGRAMMING PARADIGMS

Max.	Marks: 100 Dura	ation: 3 Hours
	PART A	3.6.1
1	Answer all questions, each carries 4 marks.  What is short circuit evaluation? Give an example.	Marks (4)
2	Differentiate between enumeration and subrange datatypes.	(4)
3	Differentiate between strongly typed and statically typed language.	(4)
4	What is a subroutine calling sequence?	(4)
5	What is the principle purpose of generics?	(4)
6	Write a code in Scheme to find factorial of a number using recursion.	(4)
7	How we can implement multiple inheritance in java?	(4)
8	Compare greedy matching with minimal matching.	(4)
9	What is a thread pool in java? What is its use?	(4)
10	What is busy waiting? What is its principal alternative?	(4)
	PART B	
11	Answer any two full questions, each carries 9 marks.	(6)
11 a		(6)
b	Write a tail recursive function to print the Fibonacci series.	(3)
12 a	How type coercion can be performed in C language? Illustrate with an example of the coercion can be performed in C language?	mple. (4)
b	Differentiate between structural equivalence and name equivalence examples.	with (5)
13 a	What is the order of evaluation in C programming language?	(4)
b	How array elements are stored in memory? Explain the memory ad calculation.	dress (5)
	PART C	
1/1 a	Answer any two full questions, each carries 9 marks.  Show the functioning of co-routines with appropriate diagram.	(3)
b		(6)
15 a		(3)
b	1 7	(6)
16 a	What is a static chain? How is it maintained during a subroutine call?	(6)
b	How equality testing can be done in Scheme?	(3)

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## PART D

		Answer any two full questions, each carries 12 marks.	
17	a)	Write a C++ program to add two complex numbers of the form a+ib using	(8)
		operator overloading and explain the overloading.	
	b)	How to implement overloading in C++?	(4)
18	a)	What do you mean by late binding of machine code? What are its advantages	(6)
		and disadvantages?	
	b)	Write short notes on Virtual Machines.	(3)
	c)	What is quasi parallelism?	(3)
19	a)	Explain busy wait synchronization.	(6)
	b)	What are the different features of scripting languages?	(6)

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## APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

## SEVENTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

## **Course Code: CS405 Course Name: COMPUTER SYSTEM ARCHITECTURE**

Max. Marks: 100 **Duration: 3 Hours** 

			PART A		
		Answer a	ll questions, each carries 4	4 marks.	Marks
1		With a neat sketch, explain	the architecture of a vecto	r supercomputer.	(4)
2		Explain implicit and explic	it parallelism in parallel pr	rogramming	(4)
3		Compare the characteristic	s of CISC and RISC Archit	tectures	(4)
4		Differentiate between cross	sbar network and multipor	t memory.	(4)
5		How does cache inconsist	ency occur in caches due	to process migration and	(4)
		I/O?			
6		Differentiate between store	and forward and wormhol	e routing	(4)
7		What are the possible hazards that can occur between read and write operations in an instruction pipeline?			(4)
8		Determine the frequency o	f the pipeline if the stage of	lelays are $\tau_1 = 3$ ns, $\tau_2 = \tau_3$	(4)
		=5ns and $\tau_4$ =8 ns and the latch delay is 1 ns.			
9		Distinguish between sta	tic dataflow computers	and dynamic dataflow	(4)
	computers.				
10		What are the four context switching polices for multithreaded architecture?			(4)
			PART B		
		•	o full questions, each carr		
11	a)	Explain Flynn's classificat	ion of computer architectur	re	(4)
	b)	A 40 MHz processor was	s used to execute a bench	hmark program with the	
		following instruction mix a	and clock cycle counts:		
		Instruction Type	Instruction count	Clock cycle count	
		Integer Arithmetic	35000	1	
		Data Transfer	20000	2	
		Floating point	15000	2	
		Control Transfer	6000	2	

Determine the effective CPI, MIPS rate and execution time for this program. (5)

12 a) Explain the terms (i) Hit Ratio (ii) Effective Access Time with proper (3) equations

b) Consider the design of a three level memory hierarchy with the following specifications for memory characteristics:

Memory level	Access time	Capacity	Cost/Kbyte
Cache	t1=25 ns	s1=512 Kbytes	c1=\$1.25
Main Memory	t2=903 ns	s2=32 Mbytes	c2=\$0.2
Disk array	t3=4 ms	s3 =39.8 Gbytes	c3=\$0.0002

Hit ratio of cache memory is h1=0.98 and a hit ratio of main memory is h2=0.9.

- (i) Calculate the effective access time.
- (ii) Calculate the total memory cost. (6)
- 13 a) Explain the role of compilers in exploiting parallelism (3)
  - b) Explain VLIW architecture. Also explain pipelining in VLIW processors. (6)

## PART C Answer any two full questions, each carries 9 marks.

- 14 a) Draw the state transition graph for a cache block using Goodman's write-once (3) protocol for cache coherence.
  - b) Design an 8 input omega network using 2X2 switches as building blocks. (6) Show the switch settings for the permutation  $\pi_1$ =(0,6,4,7,3)(1,5)(2). Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context.
- 15 a) Differentiate between synchronous and asynchronous model of linear pipeline (3) processors.
  - b) Consider the following pipeline reservation table:

	1	2	3	4
<b>S</b> 1	X			X
S2		X		
S3			X	

- i) What are the forbidden latencies?
- ii) Draw the transition diagram.
- iii) List all the simple cycles and greedy cycles.
- iv) Determine the optimal constant latency cycle and minimal average latency (MAL)

		v) Let the pipeline clock period be $\tau$ =20ns. Determine the throughput of	
		the pipeline.	(6)
16	a)	Explain full-map directory based protocol.	(4)
	b)	What do you mean by dimension order routing? Consider a 16 node hypercube	(5)
		network. Based on E-cube routing algorithm, show how to route a message	
		from 0010 to 1001. Find all intermediate nodes on routing path.	
		PART D	
		Answer any two full questions, each carries 12 marks.	
17	(a)	Explain the Tomasulo's algorithm for the dynamic instruction scheduling.	(5)
	(b)	Explain the concept of in-order issue and out-of-order issue with respect to	(7)
		superscalar processor.	
18	a)	Explain any three latency hiding techniques used in distributed shared memory	(9)
		multi computers.	
	b)	Write a short note on fine-grain parallelism.	(3)
19	a)	Explain static branch prediction strategy and dynamic branch prediction	(6)
		strategy.	
	b)	With a neat diagram explain the architecture of ETL/EM-4 dataflow	(6)
		architecture.	

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## APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SEVENTH SEMESTER B.TECH DEGREE EXAMINATION(S), MAY 2019

# Course Code: CS405 Course Name: COMPUTER SYSTEM ARCHITECTURE

Max. Marks: 100 Duration: 3 Hours

		2 #111101110	1100115
		PART A	
		Answer all questions, each carries 4 marks.	Marks
1		With proper equations, explain the terms (i) CPU Time (ii) Throughput Rate	(4)
2		Explain NUMA model for Multiprocessor Systems	(4)
3		Explain the property of locality of reference in memory.	(4)
4		A generalized multiprocessor system architecture combines features from the	(4)
		UMA, NUMA and COMA models. Justify the answer.	
5		Differentiate write-invalidate and write-update coherence protocols for write	(4)
		through caches.	
6		Explain the factors speedup, efficiency and throughput of a k-stage linear	(4)
		pipeline.	
7		Illustrate with example how internal data forwarding among multiple functional	(4)
		units can improve the throughput of a pipelined processor.	
8		With an example bring out the difference between the Carry-Save Adders (CSA)	(4)
		and Carry Propagate Adder (CPA).	
9		Explain the distributed cacheing.	(4)
10		Illustrate the scalable coherence interface (SCI) interconnect model.	(4)
		PART B	
		Answer any two full questions, each carries 9 marks.	
11	a)	What is the significance of Bernstein's conditions to detect parallelism?	(4)
	b)	Consider the execution of the following code segment consisting of seven	
		statements. Use Bernstein's conditions to detect the maximum parallelism	
		embedded in this code. Justify the portions that can be executed in parallel and	
		the remaining portions that must be executed sequentially. Rewrite the code	
		using parallel constructs such as Cobegin and Coend. No variable substitution is	
		allowed. All statements can be executed in parallel if they are declared within	

the same block of a (Cobegin and Coend) pair.

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		S1: $A=B+C$	
		S2: $C=D+E$	
		S3: $F=G+E$	
		S4: $C=A+F$	
		S5: $M=G+C$	
		S6: $A=L+E$	
		S7: $A=E+A$	(5)
12	a)	Explain memory hierarchy.	(3)
	b)	You are asked to perform capacity planning for a two-level memory system. The	
		first level, M <sub>1</sub> , is a cache with three capacity choices of 64 Kbytes, 128 Kbytes,	
		and 256 Kbytes. The second level, $M_2$ , is a main memory with a 4-Mbyte	
		capacity. Let $c_1$ and $c_2$ be the cost per byte and $t_1$ and $t_2$ the access times for $M_1$	
		and $M_2$ respectively. Assume $c_1$ =20 $c_2$ and $t_2$ =10 $t_1$ . The cache hit ratios for the	
		three capacities are assumed to be 0.7, 0.9 and 0.98 respectively.	
		(i) What is the average access time $t_a$ in terms of $t_1$ =20 ns in the three cache	
		designs? (Note that $t_1$ is the time form CPU to $M_1$ and $t_2$ is that from CPU	
		to $M_2$ )	
		(ii) Express the average byte cost of the entire memory hierarchy if	
		$c_2 = $0.2/Kbyte.$	(6)
13	a)	Explain SIMD machine model.	(3)
	b)	Explain Superscalar architecture. Also explain pipelining in superscalar	
		processors.	(6)
		PART C	
1 4		Answer any two full questions, each carries 9 marks.	(2)
14	a)	Explain hot spot problem.	(3)
	b)	Design an 8 input omega network using 2X2 switches as building blocks. Show	(6)
		the switch settings for the permutations $\pi_1=(0,7,6,4,2)(1,3)(5)$ . Show the	
		conflicts in switch settings, if any. Explain blocking and non-blocking networks	
		in this context.	
15	a)	Differentiate between linear and nonlinear pipeline processor.	(3)
	b)	Consider the following pipeline reservation table:.	

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	1	2	3	4	5	6
<b>S</b> 1	X					X
S2		X			X	
<b>S</b> 3			X			
S4				X		
S5		X				X

- i) What are the forbidden latencies?
- ii) Draw the transition diagram.
- iii) List all the simple cycles and greedy cycles.
- iv) Determine the optimal constant latency cycle and minimal average latency (MAL)
- v) Let he pipeline clock period be  $\tau$ =20ns. Determine the throughput of the pipeline.

(6)

- 16 a) Explain write- invalidate snoopy protocol using write back policy. (4)
  - b) Explain various message routing schemes used in message passing multicomputers. (5)

# PART D Answer any two full questions, each carries 12 marks.

- 17 a) Explain in detail the effect of branching and various branch handling strategies. (9)
  - b) Explain the scoreboarding scheme employed by the CDC 6600 processor. (3)
- 18 a) With a neat diagram explain the architecture of a multiple context processor (6) model.
  - b) What are the problems of asynchrony and their solutions in massively parallel (6) processors?
- 19 a) Compare the design and performance of a superpipelined and superpipelined (6) superscalar processors.
  - b) With a neat diagram explain the MIT/Motorola \*T prototype multithreaded (6) architecture.

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SEVENTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

**Course Code: CS405** 

Course Name: COMPUTER SYSTEM ARCHITECTURE Max. Marks: 100 **Duration: 3 Hours** PART A Answer all questions, each carries 4 marks. Marks 1 A 400MHz processor was used to execute a program with 150000 floating point (4) instructions with clock cycle count of 1. Determine the execution time and MIPS rate for this program. 2 State Amdahl's law. Write an expression for the overall speed up. (4) 3 Distinguish between scalar RISC and super-scalar RISC in terms of instruction (4) issue, pipeline architecture and performance. 4 Discuss the schematic representation of a generalized multiprocessor system. (4) 5 Explain chained cache coherence protocol. (4) 6 Consider the execution of a program of 15,00,000 instructions by a linear pipeline (4) processor with a clock rate of 1000 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per cycle. The penalties due to branch instruction and out-of-order execution are ignored. a) Calculate the speedup factor in using this pipeline to execute the program as compared with the use of an equivalent non-pipelined processor with an equal amount of flow-through delay. b) Find out the efficiency and throughput of this pipelined processor. 7 Write short notes on internal data forwarding. (4) 8 Explain Goodman's write once protocol with transition diagram. (4) 9 List any two advantages and disadvantages of Scalable Coherence Interface(SCI). (4) What are the four context switching policies adopted by multithreaded 10 (4) architectures? **PART B** Answer any two full questions, each carries 9 marks. Discuss the Bernstein's conditions for checking the parallelism among a set of 11 a) (3) processes.

Analyze the data dependences among the following statements and construct a

(6)

b)

dependency graph. Also detect the parallelism embedded in them.

S1: Load R1, M(100) / R1 ← Memory(100) / S2: Move R2, R1 / R2 ← (R1) / S3: Inc R1 / R1 ← (R1) + 1 / S4: Add R2, R1 / R2 ← (R2) + (R1) / S5: Store M(100), R1 / Memory(100) ← (R1) /

- a) Define the inclusion property of a memory hierarchy. Illustrate the data transfers (5) between adjacent levels of a memory hierarchy.
  - b) Consider a two-level memory hierarchy, M1 and M2 of sizes 64Kbytes and (4) 4Mbytes respectively, with access time t1 = 20ns and t2 = 200ns and costs c1 and c2 are \$0.01/byte, c2 = \$0.0005/byte respectively. The cache hit ratio h1 = 0.95 at the first level. Find the effective access time and total cost of this memory system.
- Differentiate between the following with necessary diagrams:
  - a) UMA and NUMA multiprocessor models. (4)
  - b) RISC and CISC (5)

### **PART C**

## Answer any two full questions, each carries 9 marks.

- 14 a) Explain the different levels of hierarchy of bus systems. (4)
  - b) Define the write-invalidate snoopy bus protocol for maintaining cache coherence. (5) Show the different possible state transitions for write-through and write-back cache using the write-invalidate protocol.
- 15 Consider the five-stage pipelined processor specified by the following reservation table and answer the following: (S indicate the stages)

	1	2	3	4	5	6
<b>S1</b>	Х					Х
S2		Х		Х		
S3			Х			
S4				Х	Х	

- (i) List the set of forbidden latencies and the collision vector.
- (ii) Draw the state transition diagram showing all possible initial sequences without causing a collision in the pipeline. (3)

(2)

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		(iii) List all the simple and greedy cycles from the state diagram.	(2)
		(iv) Determine the minimal average latency (MAL).	(2)
16	a)	Explain the three major operational characteristics of a multiprocessor	(3)
		interconnection network.	
	b)	Analyse and compare the communication latencies of Store-and Forward and	(3)
		Wormhole routing schemes.	
	c)	Consider a 16-node hypercube network. Based on the E-cube routing algorithm,	(3)
		show how to route a message from node (0111) to node (1101). All intermediate	
		nodes must be identified on the routing path.	
		PART D	
		Answer any two full questions, each carries 12 marks.	
17	a)	Which are the three logic hazards possible in an instruction pipeline? Define each.	(6)
		Write the necessary conditions for each to occur.	
	b)	Explain the in-order and out-of-order pipeline scheduling policies for a superscalar	(6)
		machine with an example.	
18	a)	Explain the importance of Tomasulo's algorithm for dynamic instruction	(8)
		scheduling.	
	b)	What do you mean by Release Consistency (RC) memory model? Give the	(4)
		conditions to ensure RC.	
19	a)	Explain the effect of branching in instruction pipelining. Find the execution time	(6)
		and throughput of the pipeline for n instructions by considering the effect of	
		branching. How branch penalty is reduced using delayed branch strategy.	
	b)	Explain any two latency hiding techniques used in distributed shared memory	(6)
		multi computers.	

Seventh semester B.Tech examinations (S), September 2020

## Course Code: CS405 Course Name: COMPUTER SYSTEM ARCHITECTURE

Max. Marks: 100 Duration: 3 Hours PART A Answer all questions, each carries 4 marks. Marks 1 With neat sketch differentiate explicit and implicit parallelism. **(4)** 2 Explain COMA model for Multiprocessor Systems. **(4)** 3 Define a) Instruction issue latency b) Instruction issue rate. (4) 4 Explain the significance of multiport memory. (4) 5 How hardware synchronization can be achieved in a multiprocessor system. (4) 6 Explain different message routing schemes. (4) 7 What is meant by pipeline stalling? (4) 8 Differentiate between Carry save adder (CSA) and Carry propagation adder **(4)** (CPA). 9 Suggest different methods to overcome asynchrony problem. (4) 10 Explain distributed caching. (4) PART B Answer any two full questions, each carries 9 marks. 11 a) Define Amdahl's Law. (3) b) Consider the execution of an object code with 200,000 instructions on a 40-(6) MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment.

Instruction type	CPI	Instruction mix
Arithmetic and logic	1	56%
Load/store with cache hit	2	22%
Branch	4	10%
Memory reference with cache miss	8	12%

Calculate the average CPI, MIPS rate and Execution time.

12 a) Compare RISC and CISC scalar processor architectures.

**(4)** 

b) Consider the design of a three-level memory hierarchy with the following (5) specifications for memory characteristics:

Memory Access		Capacity	Cost/Kbyte
Level	time		
Cache	t1=20ns	s1=512Kbytes	c1=\$1.30
Main Memory	t2=905ns	s2=32Mbytes	c2=\$0.2
Disk array	t3=5ms	s3=40Gbytes	c3=\$0.0003

Hit ratio of cache memory is h1=0.98 and a hit ratio of main memory is h2=0.9.

- (i) Calculate the effective access time.
- (ii) Calculate the total memory cost.
- 13 a) State and explain Bernstein's conditions for parallelism? (3)
  - b) Detect parallelism in the following code using Bernstein's conditions. Assume (6) there are sufficient numbers of resources available.

P1: C=D\*E

P2: M=G+C

P3: A=B+C

P4: C=L+M

P5: F=G/E

## PART C

## Answer any two full questions, each carries 9 marks.

- a) Design an 8 input omega network using 2X2 switches as building blocks. Show the switch settings for the permutation π1=(0,6,3,2,5)(1,4). Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context.
  - b) Draw the two state transition graphs for a cache block using write -invalidate (3) write -through snoopy bus protocol.
- 15 a) With suitable diagram explain different flow control strategies for resolving a (4) collision between two packets.
  - b) Consider the following pipeline reservation table. (5)

	1	2	3	4
S1	X			
S2		X		X
S3			X	

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		i) What are the forbidden latencies?	
		ii) Draw the transition diagram.	
		iii) List all the simple cycles and greedy cycles.	
		iv) Determine the optimal constant latency cycle and minimal average latency	
		(MAL).	
		v) Let the pipeline clock period be $\tau$ =10ns. Determine the throughput of the	
		pipeline.	
16	a)	Compare full map directories with limited directories.	(4)
	b)	Explain E-cube routing. Consider a 64 -node hypercube network. Based on E-	(5)
		cube routing algorithm, show how to route a message from 101101 to 011010.	
		Find all intermediate nodes on routing path.	
		PART D	
		Answer any two full questions, each carries 12 marks.	
17	a)	Explain the importance of Tomasulo's algorithm for dynamic instruction	(6)
		scheduling.	
	b)	Describe the various mechanisms for improving the performance of instruction	(6)
		pipeline.	
18	a)	Explain various latency hiding techniques.	(8)
	b)	Differentiate between static and dynamic data flow computers.	(4)
19	a)	Explain various branch prediction techniques.	(6)
	b)	With suitable diagrams explain ETL/EM-4 architecture.	(6)
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## APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SEVENTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: CS407 Course Name: DISTRIBUTED COMPUTING

Max. Marks: 100 Duration: 3 Hours

### PART A Answer all questions, each carries 4 marks. Marks 1 List any 4 issues in the design of a distributed system. **(4)** 2 What is the need of safety and liveness as requirements in an Election (4) algorithm? 3 Explain the key techniques used for indirect communication. **(4)** 4 Why Skype is called an Overlay network? **(4)** Evaluate the performance of Maekawa's voting algorithm with respect to fault 5 (4) tolerance Why is "send group" group communication primitive preferred over "send" 6 **(4)** primitive? 7 What is the difference between two-phase locking and strict two-phase locking **(4)** in transactions? 8 What do you mean by Vice and Venus in AFS?. What are their roles? **(4)** 9 State the rules for committing of nested transactions. **(4)** 10 Define mobile agents. How can they be potential security threats? **(4)** PART B Answer any two full questions, each carries 9 marks. What are the two variants of the interaction model in distributed systems? On 11 **(4)** what points do they differ? b) Describe any 4 key architectural patterns used in distributed systems. (5) 12 a) List and explain the different types of communication paradigms used within (6) distributed systems. b) A distributed system is defined as one in which hardware or software (3) components located at networked computers communicate and coordinate their actions only by passing messages, What are the consequences of defining a distributed system in this manner?

Write notes on mobile and ubiquitous computing.

13 a)

D		R7986 Pages	Pages: 2	
	b)	Compare work station server model with processor pool model.	(5)	
		PART C		
1.4	,	Answer any two full questions, each carries 9 marks.	(6)	
14	a)	Describe IP multicast in detail	(6)	
1.5	b)	Give notes on failure model for multicast datagrams.	(3)	
15	a)	Explain the implementation of RPC mechanism with a neat diagram.	(4)	
1.6	b)	Summarize any five Distributed File System requirements.	(5)	
16	a)	Explain NFS Architecture with diagram	(5)	
	b)	Differentiate Andrew file system and NFS	(4)	
		PART D  Answer any two full questions, each carries 12 marks.		
17	a)	Explain the lost update and inconsistent retrievals problems in concurrent	(6)	
		transactions with the help of examples.		
	b)	Why serial equivalence requires that once a transaction has released a lock on an	(6)	
		object, it is not allowed to obtain any more locks. A server manages the objects		
		a1, a2,, an. The server provides two operations for its		
		clients: read (i) returns the value of ai;		
		write(i, Value)assigns Value to ai.		
		The transactions $T$ and $U$ are defined as follows:		
		T: x = read(j); y = read(i); write(j, 44); write(i, 33);		
		U: x = read(k); write(i, 55); y = read(j); write(k, 66).		
		Describe an interleaving of the transactions T and U in which locks are released		
		earlywith the effect that the interleaving is not serially equivalent.		
18	a)	Describe a deadlock detection scheme for a single server with an example.	(6)	
	b)	Write an algorithm to implement mutual exclusion between N processes that is	(6)	
		based upon multicast and logical clocks. Illustrate the algorithm using the		
		situation involving three processes p1,p2, p3.		
19		With an example and suitable figure describe the operation of bully algorithm.	(12)	
		Justify whether it meets the requirements of election, during run of the		
		algorithm. Also evaluate the performance of the above algorithm.		

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SEVENTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

Course Code: CS407

**Course Name: DISTRIBUTED COMPUTING** 

Max. Marks: 100 Duration: 3 Hours

### **PART A**

## Answer all questions, each carries 4 marks.

Marks

- Explain network transparency. The e-mail addresses ensures network (4) transparency, justify.
- 2 Compare tightly coupled and loosely coupled systems with neat diagrams. (4)
- 3 Illustrate the following placement strategies used in a distributed system. (4)
  - i. mapping of services to multiple servers / proxy servers
  - ii. mobile code
- What impact does the introduction of overlay networks have on the traditional (4) Internet architecture, and in particular on the programmer's conceptual view of the Internet?
- 5 Explain the directory service and its interface operations in a file service (4) architecture.
- 6 Illustrate the iterative navigation process in name resolution with a neat diagram. (4)
- The operation create inserts a new bank account at a branch. The transactions T (4) and U are defined as follows:

*T*: *aBranch.create("Z")*;

U: z.deposit(10); z.deposit(20).

Assume that Z does not yet exist. Assume also that the deposit operation does nothing if the account given as the argument does not exist. Consider the following interleaving of transactions T and U:

T	U
	z.deposit(10);
aBranch.create(Z);	
	z.deposit(20);

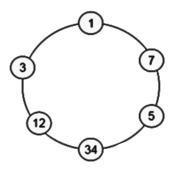
State the balance of Z after their execution in this order. Are these consistent with serially equivalent executions of T and U?

8 What is a deadlock? Illustrate the various ways of detecting deadlock in a (4)

9		distributed environment.  Illustrate the working of central server algorithm with a diagram.	(4)
10		Explain the case of deadlock in Maekawa's voting algorithm.	(4)
10			(+)
		PART B Answer any two full questions, each carries 9 marks.	
11	a)	Illustrate the processor-pool model with a neat diagram. How is it different from	(5)
		workstation-server model?	
	b)	Describe the heterogeneity and scalability issues in distributed computing.	(4)
12	a)	Explain distributed computing as a 'Utility'.	(4)
	b)	Identify the different threats to communication channels and explain different	(5)
		mechanisms to overcome that.	
13	a)	Explain the different categories of failures in a distributed environment.	(6)
	b)	Outline three specific and contrasting examples of the increasing levels of	(3)
		heterogeneity experienced in contemporary distributed systems.	
		PART C	
14	a)	Answer any two full questions, each carries 9 marks.  With a neat diagram, explain the tasks in group membership management.	(5)
	b)	Describe the multicast support provided in IPv4.	(4)
15	a)	With a neat diagram, illustrate the implementation of RPC.	(5)
	b)	Summarize the distributed file system requirements.	(4)
16	a)	Sketch the architecture of Sun NFS and explain the role of different components.	(6)
	b)	Distinguish between whole file serving and whole file caching in Andrew file	(3)
		system.	
		PART D	
		Answer any two full questions, each carries 12 marks.	
17	a)	Outline the lock implementation in distributed environment.	(6)
	b)	Explain dirty read and premature write problems associated with transactions	(6)
		with suitable examples.	
18	a)	What are nested transactions? Summarize the rules for committing of nested	(5)
		transactions.	
	b)	Explain the steps in Maekawa's voting algorithm.	(7)

19 a) In the ring topology shown below, if process with identifier 7 initiates election, (8) explain the election process and show the modifications happening to the election message as it passes through all the processes.

How many election and elected messages will be passed so that the coordinator be elected and known to all the processes?



b) Examine whether the Bully algorithm meets the necessary conditions for (4) election.

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SEVENTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), MARCH 2020

Course Code: CS407 Course Name: DISTRIBUTED COMPUTING Max. Marks: 100 **Duration: 3 Hours PART A** Answer all questions, each carries 4 marks. Marks 1 Define mobile agents. How this will create security threats. (4) 2 Outline the layered and tiered architectural patterns used in distributed systems. (4) 3 Distinguish between the two variants of the interaction model in distributed (4) systems. 4 Explain the three RPC call semantics. (4) 5 What is file group? How will you generate a unique identifier for a file group? **(4)** 6 Explain the mount service in NFS. (4) 7 Suppose that there are 100 items currently in a stock. Given two transactions U (4) and V as below. Explain the inconsistent retrievals problem in this scenario and propose a solution for that. U Purchase 200 items Read item count in Stock Sell 50 items 8 Explain two version locking. (4) 9 Define mutual exclusion and summarize its three essential requirements. (4) 10 Evaluate the performance of Maekawa's voting algorithm. (4) PART B Answer any two full questions, each carries 9 marks. 11 "The absence of these two transparencies most strongly affects the utilization of (4) a) distributed resources". Identify and explain the above two types of transparencies with examples. b) Compare workstation model with workstation-server model. (5) 12 a) Distinguish between mobile computing and ubiquitous computing. (4) Compare client-server architecture with peer to peer architecture. (5) b)

(4)

Distinguish between Omission Failures and Arbitrary failures.

13 a)

Outline two scenarios where the election condition E1 is broken in case of Bully

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(8)

(4)

Give an example for the execution of the algorithm to show that processes are

not necessarily granted entry to the critical section in happened-before order.

Illustrate bully algorithm for election with an example.

19 a)

algorithm.