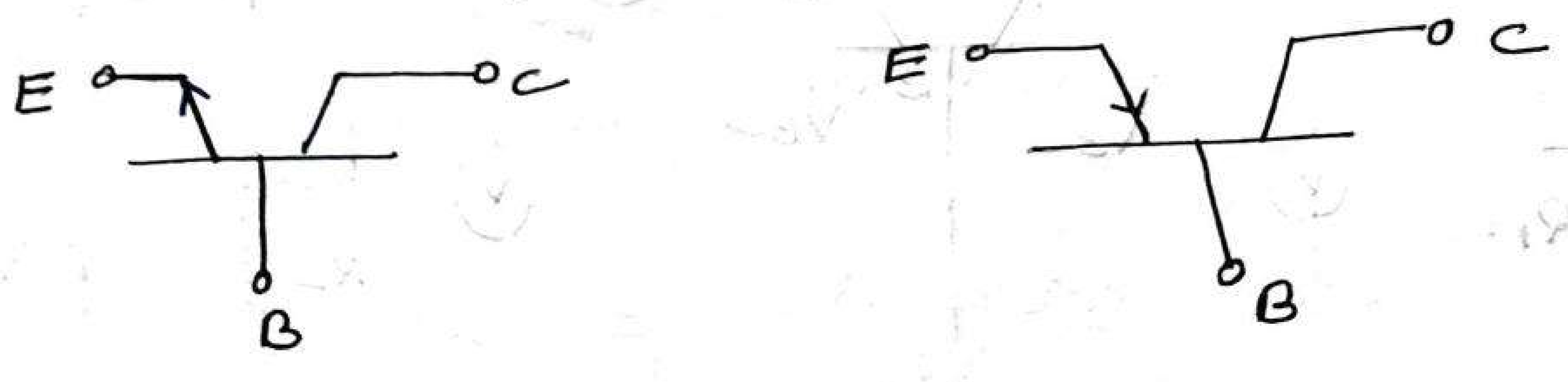
BJT { Bipolar Junction Transistor)

2 types npn transistor & pnp transistor



npn pnp

3 terminals ⇒ Emitter (E), Base (B), collector (C)

Emitter = heavily doped, moderate surface area

Base = Lightly doped, small surface area

collector = Moderately doped, large surface area

configuration ⇒ 1) common base
2) Common emitter
3) Common collector

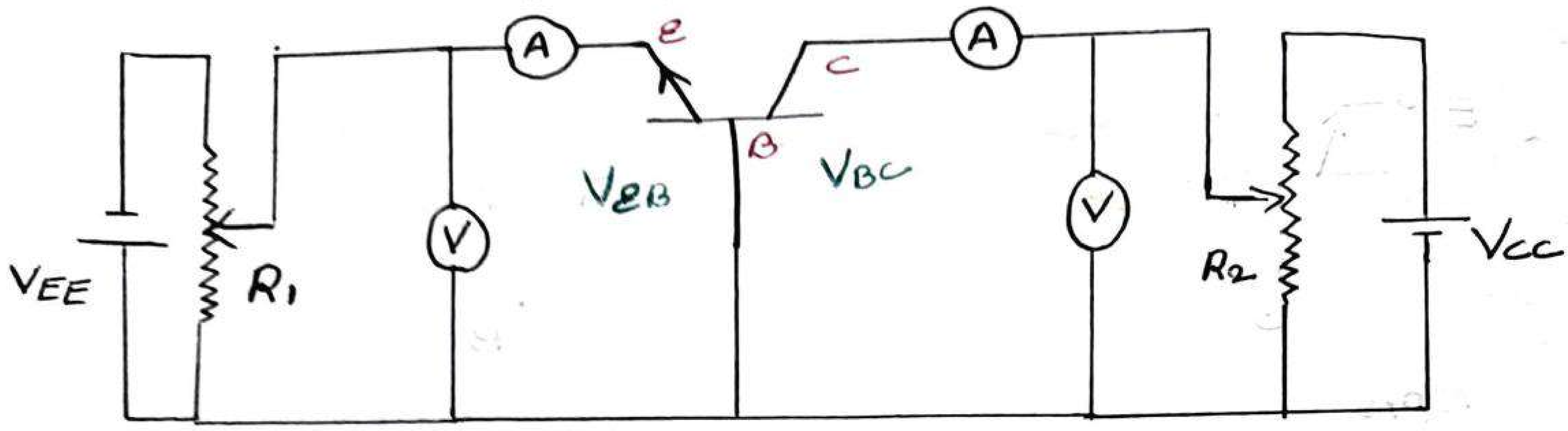
In a transistor there are two types of characteristics. they are

1) i/p characteristics = relationship b/w i/p current & i/p Voltage at const. o/p Voltage

2) o/p characteristics = relationship b/w o/p current & o/p voltage at cons. i/p current

Common Base Configuration

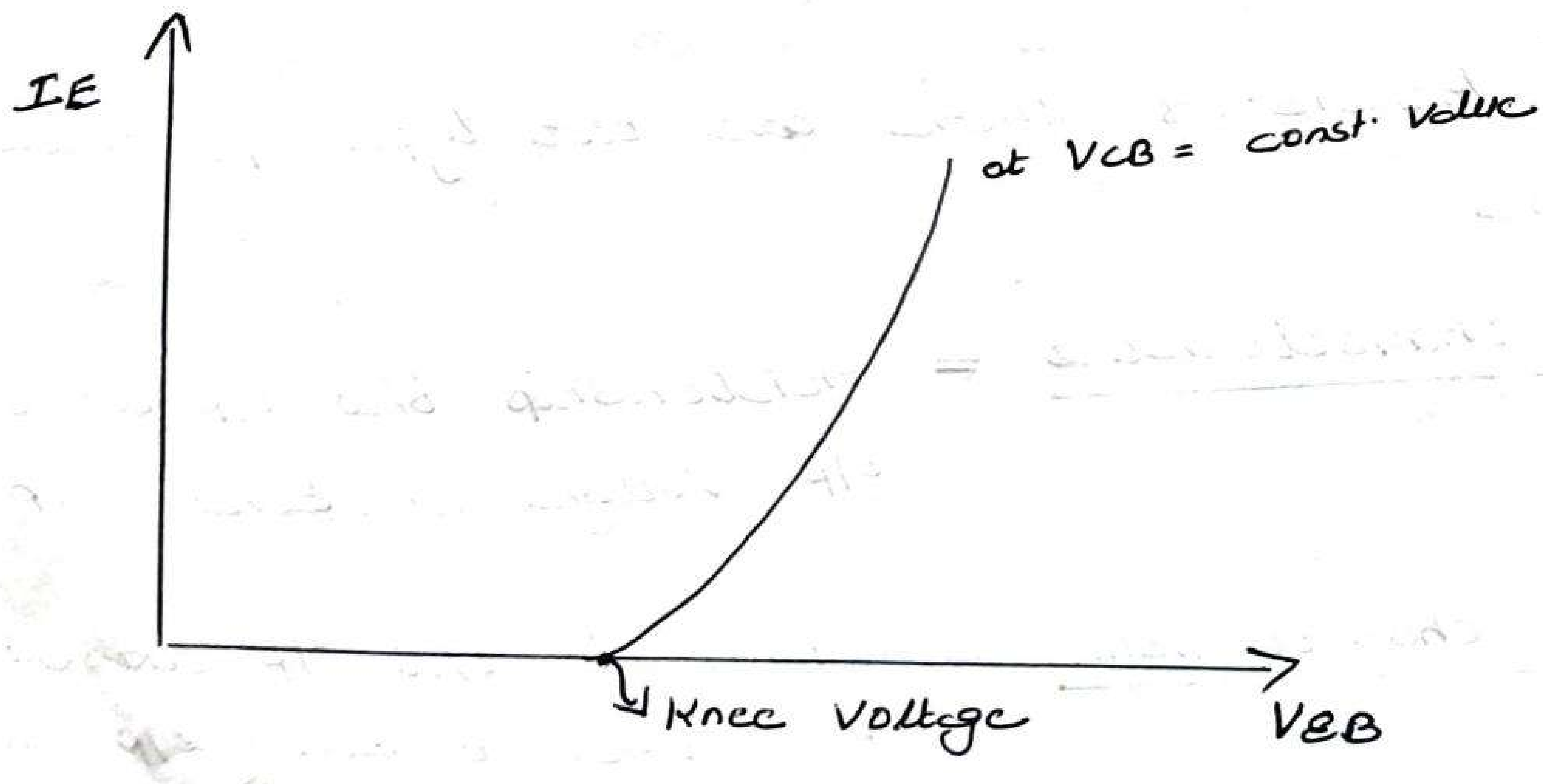
Here base is common to o/p & i/p



i/p chara

First adjust V_{CB} (o/p voltage) to a fixed value, then adjust R_1 & take ammeter & voltmeter readings. Plot a graph with V_{EB} (i/p voltage) & I_E (i/p current)

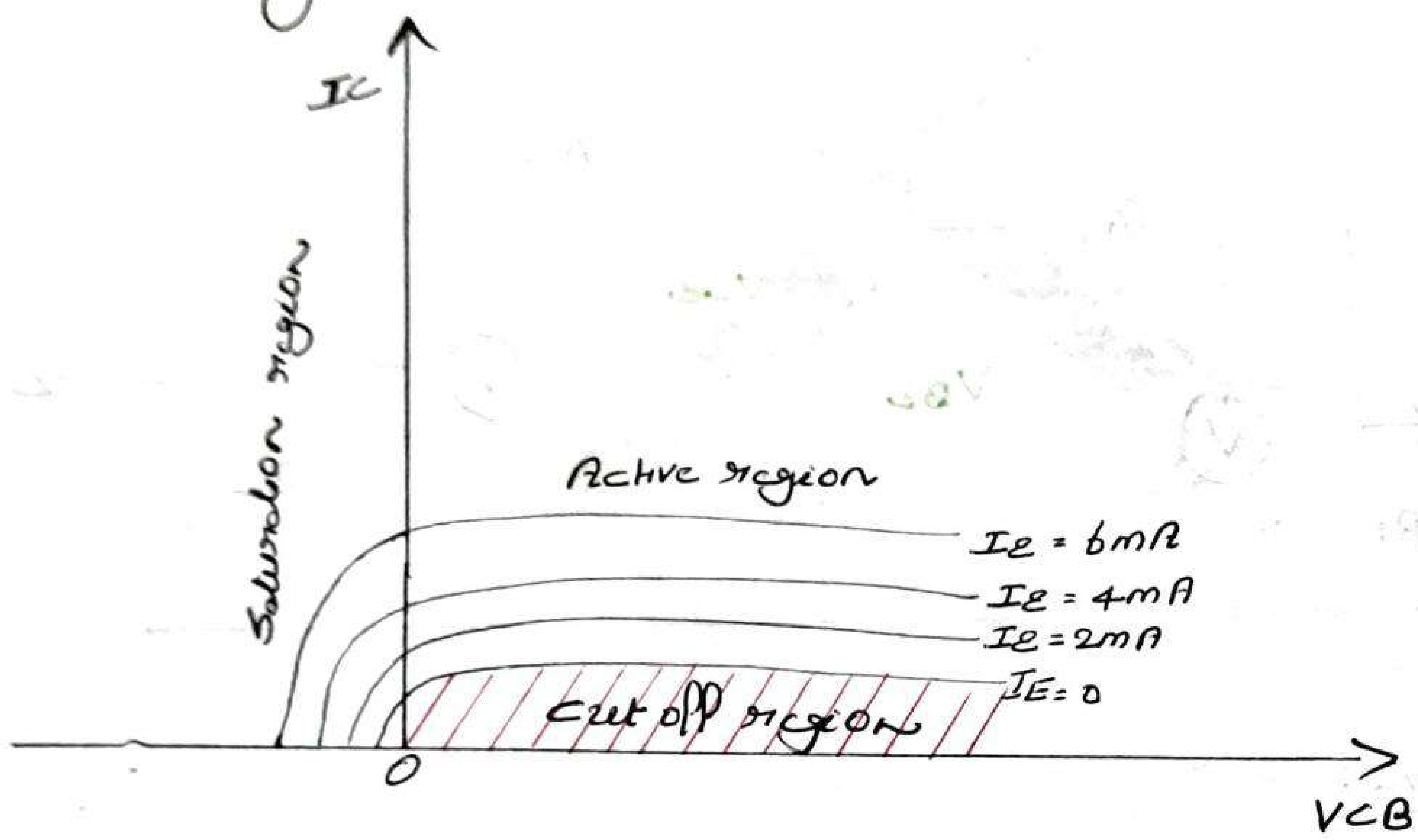
The voltage at which, current just starts flowing is called Knee voltage, it is 0.5 V for silicon & 0.1 V for germanium



i/p resistance $R_i = \dfrac{\Delta V_{EB}}{\Delta I_E}$.

O/P chara

Keeping I_E (i/p current) at constant value, increase V_{CB} & corresponding I_C is measured. Plot a graph with V_{CB} along X-axis & I_C along Y-axis.



The curve may be divided into 3 main regions.

a) Saturation region

It is on left of vertical line. In this region a small change in V_{CB} cause large variation in I_C

b) Active region

It is on right of vertical line.

c) Cut off region

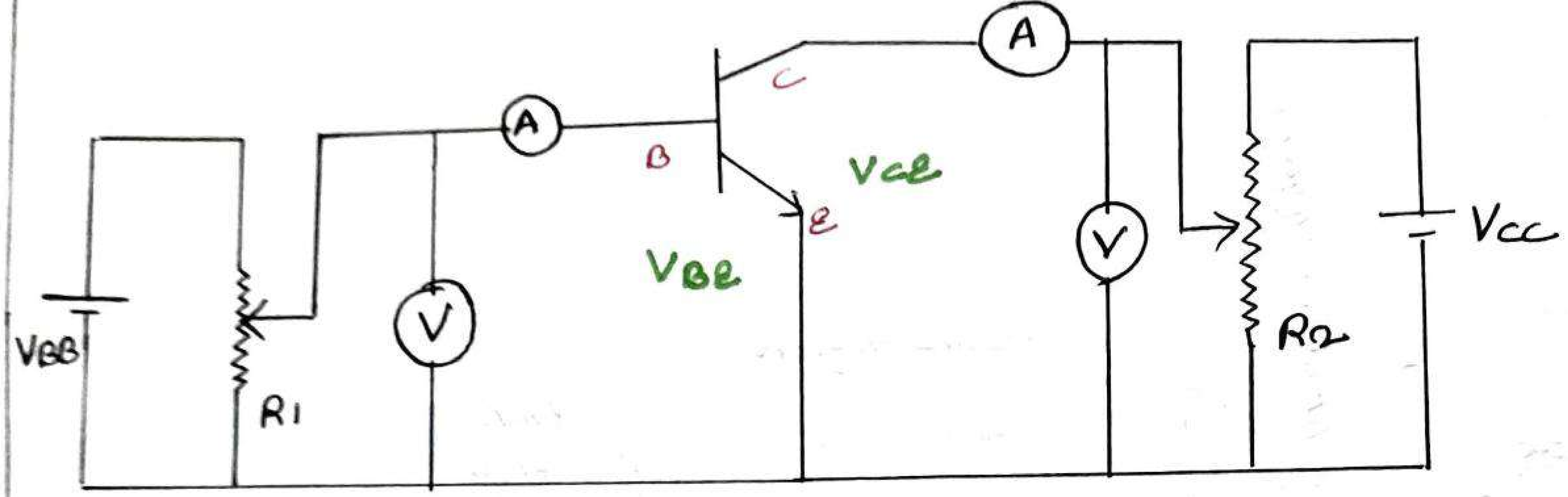
It is the shaded portion. In this region both junctions are reverse biased.

o/p resistance $R_o = \frac{\Delta V_{CB}}{\Delta I_C}$

Current amplification factor $(\alpha) = \frac{\Delta I_C}{\Delta I_E}$.

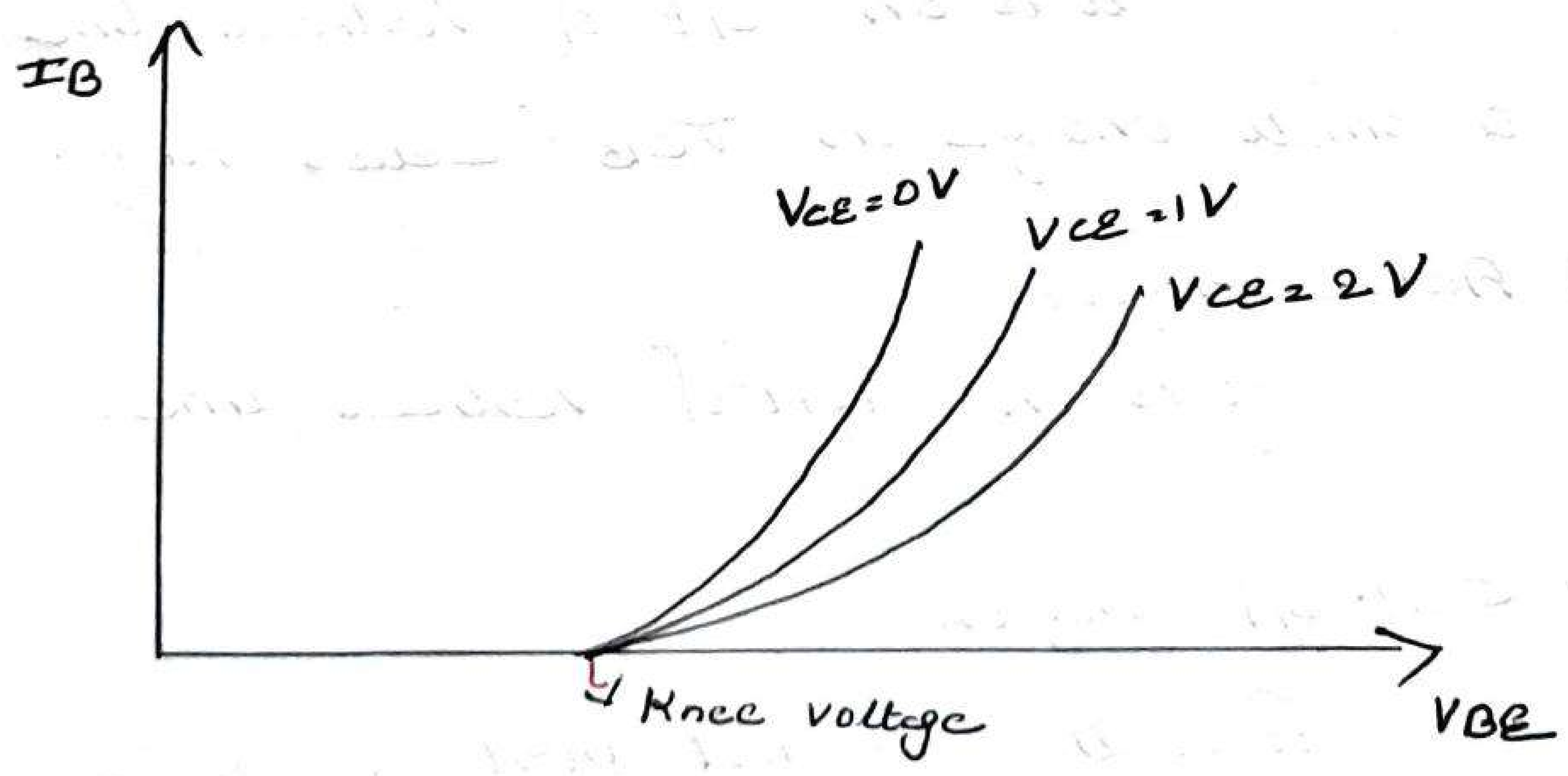
Common Emitter Configuration

Here emitter is common to o/p & i/p



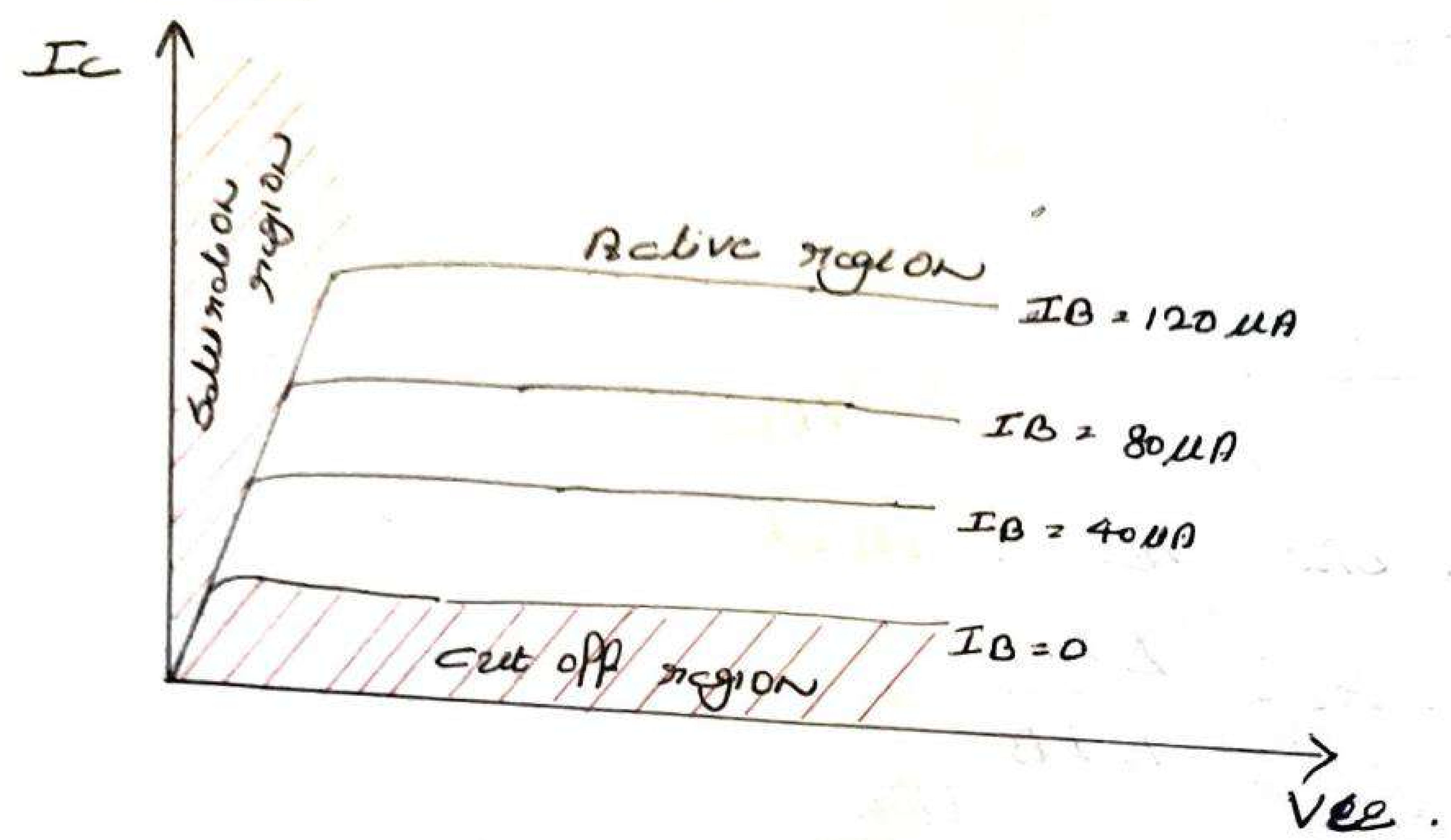
i/p chara:

V_{CE} is kept const, Then increase V_{BE} & I_B is noted.
Plot graph with V_{BE} along X-axis & I_B along Y-axes.



i/p resistance $R_i = \frac{\Delta V_{BE}}{\Delta I_B}$ at const V_{CE}

o/p chara



Adjust IB to const. value. Then increase Vce & corresponding Ic is noted.

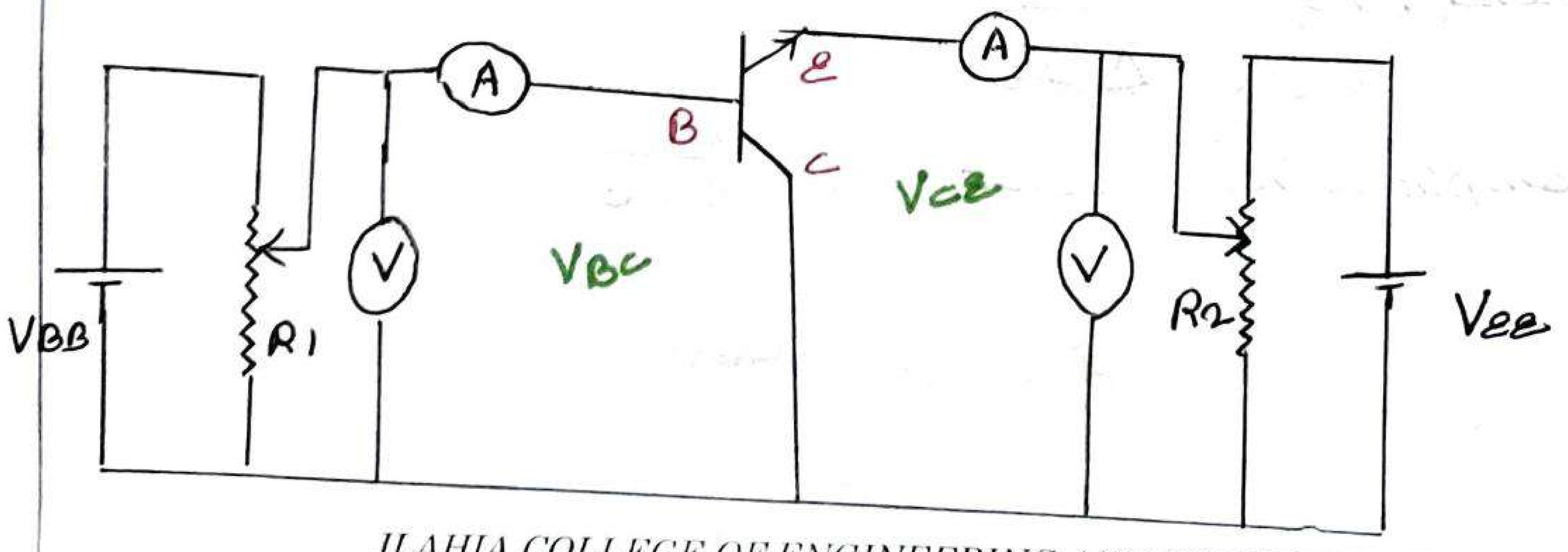
The chara has 3 main regions, active, saturation & cut-off
when $I_B = 0$, there is Ic called leakage current.

o/p resistance, $R_o = \frac{\Delta V_{CE}}{\Delta I_C}$

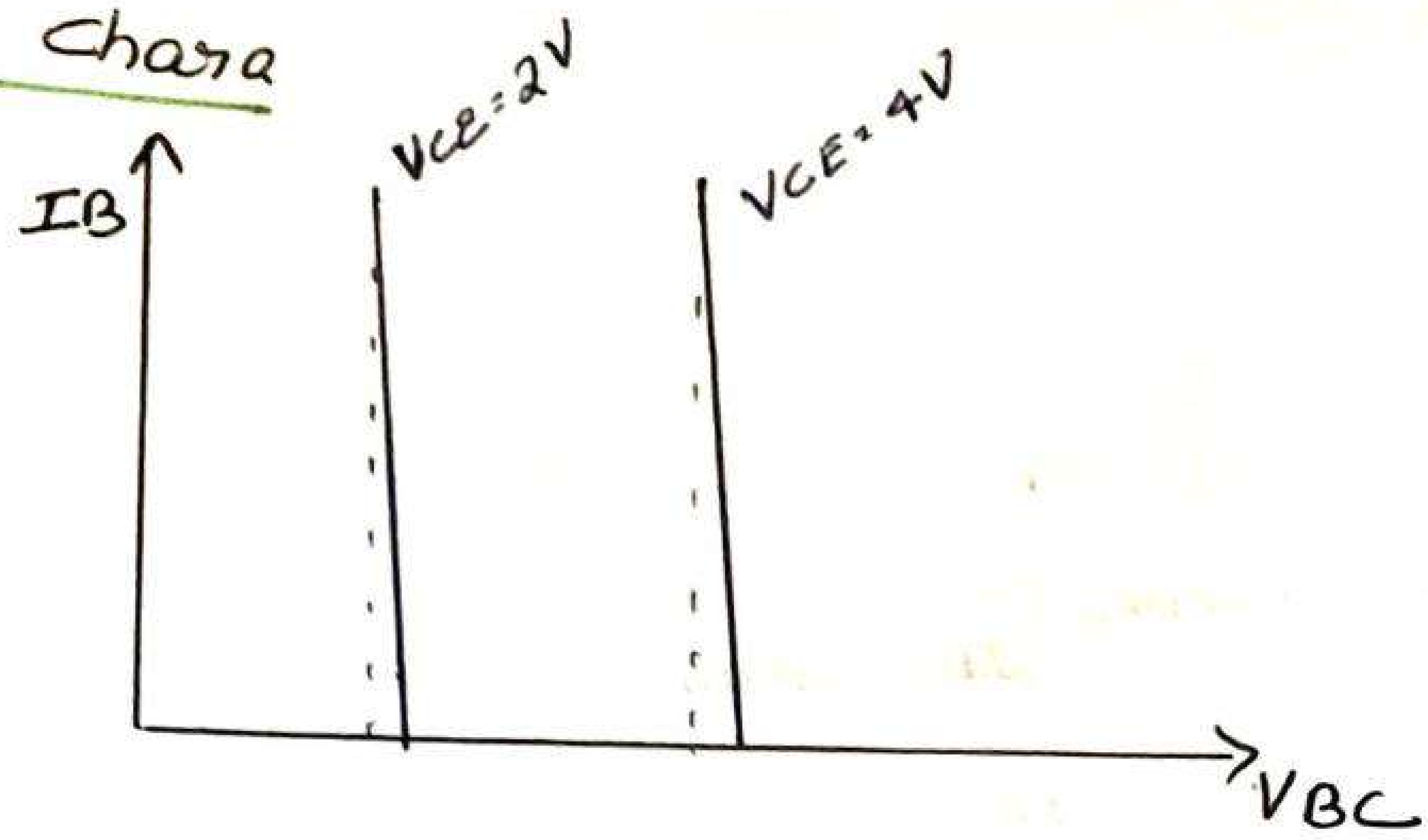
current amplification factor, $\beta = \frac{\Delta I_C}{\Delta I_B}$

Common Collector Configuration

Collector is common to o/p & i/p.



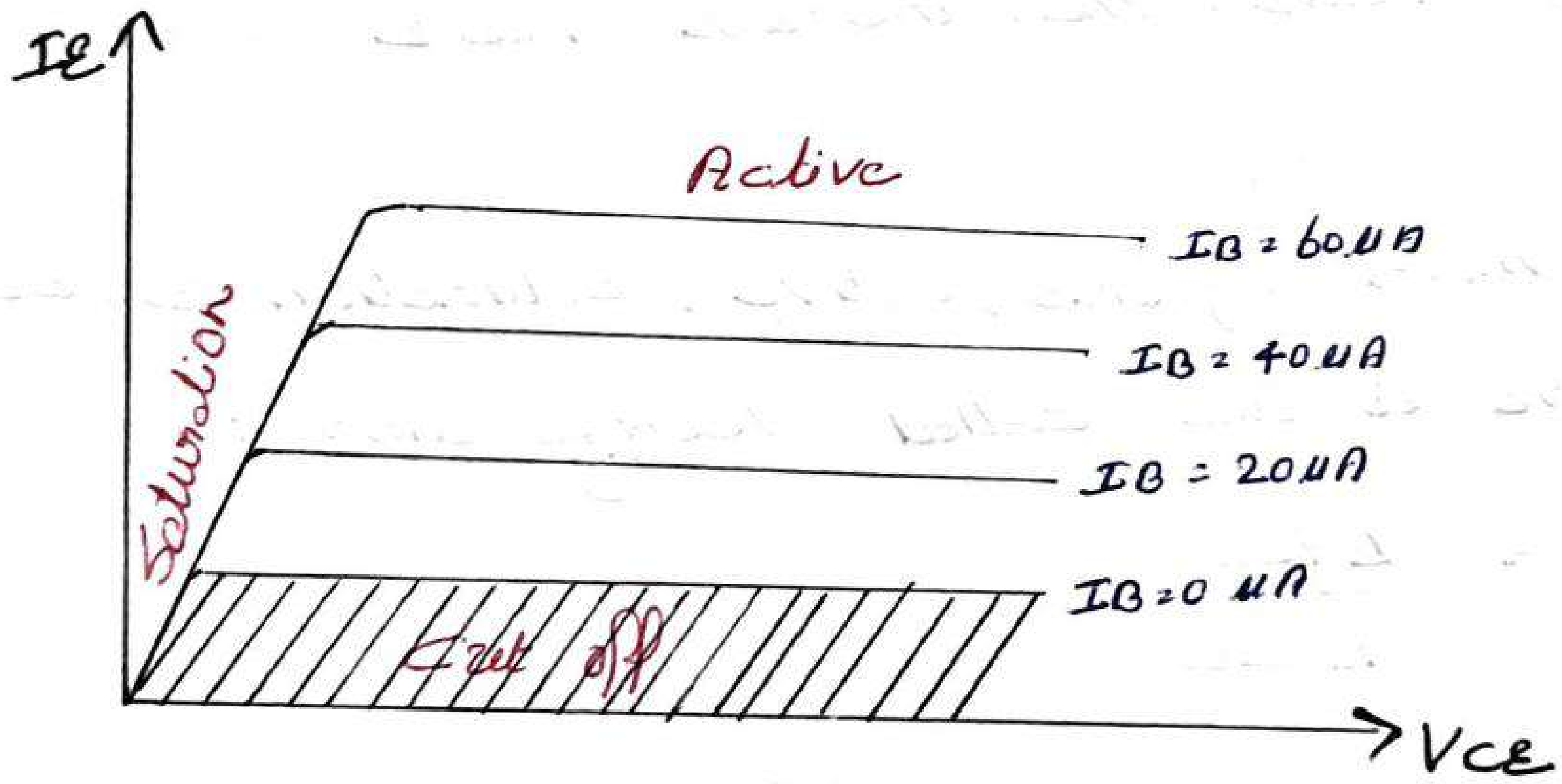
i/p chara



It is the graph b/w V_{BC} & I_B at const. V_{CE}.

i/p resistance, $R_i = \frac{\Delta V_{BC}}{\Delta I_B}$ at const. V_{CE}.

o/p chara



I_B is adjusted to const. value. Vary V_{CE} & corresponding increase in I_E is noted.

o/p resistance, $R_O = \frac{\Delta V_{CE}}{\Delta I_E}$ at const. I_B

Current amplification factor, $\gamma = \frac{\Delta I_E}{\Delta I_B}$

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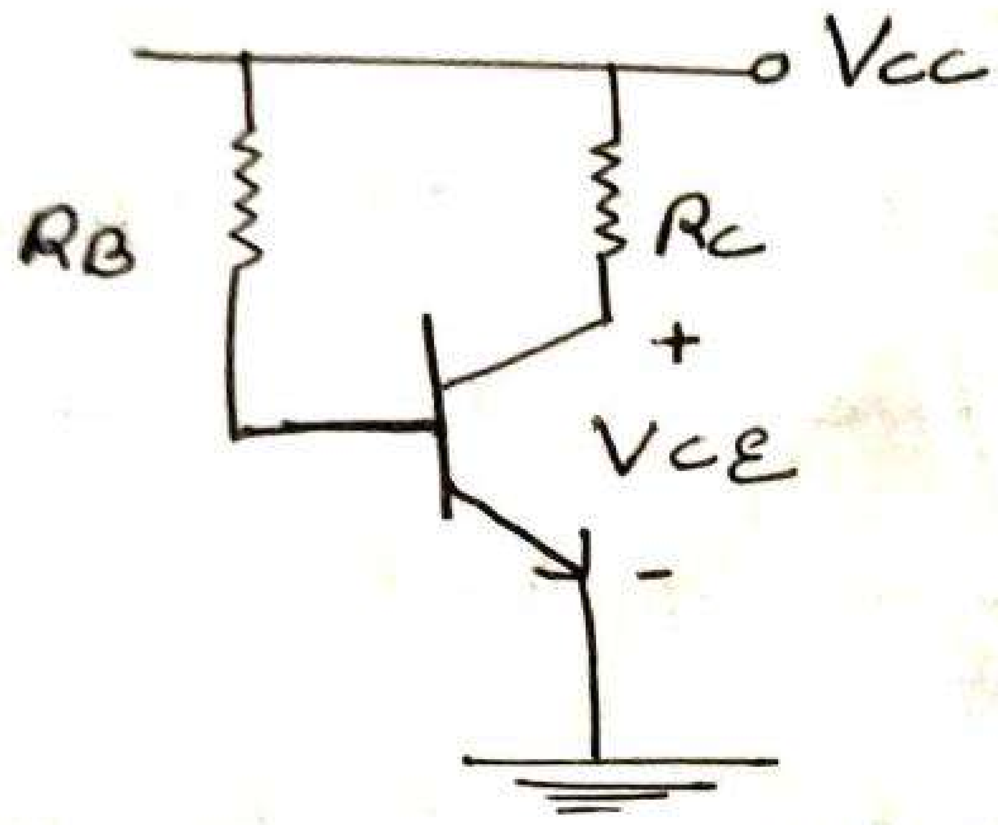
Transistor Load Lines

It is a line on which the operating point moves when the ac signal is applied to the transistor

DC load line:-



It is drawn without any ac i/p signal.

$V_{cc} = I_cR_c + V_{CE}$

$V_{CE} = V_{cc} - I_cR_c$ —— (1)

Put $V_{CE} = 0$ in eqn (1)

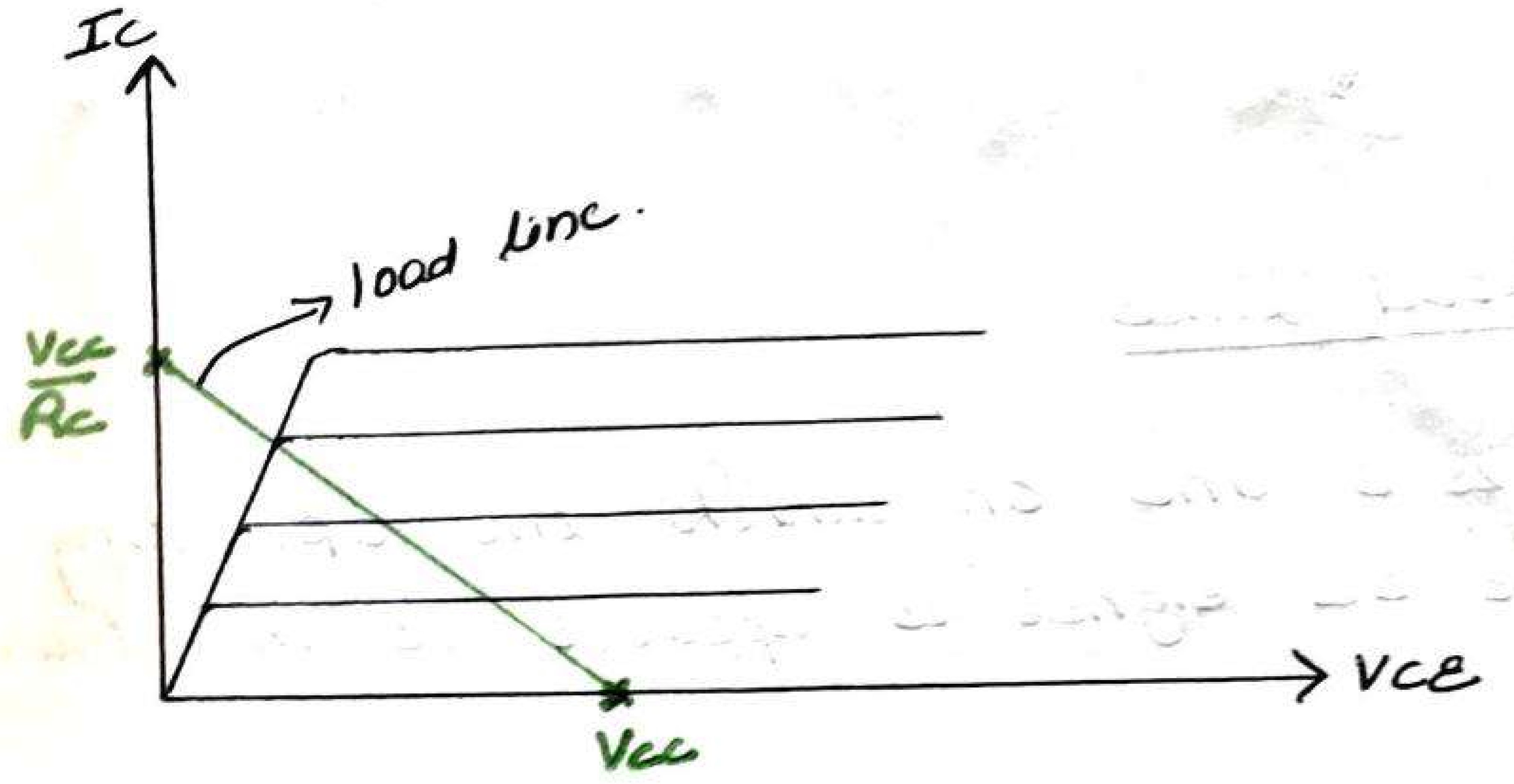
$V_{cc} = I_cR_c$

$\therefore I_c = V_{cc}/R_c$

Put $I_c = 0$ in eqn (1)

$V_{CE} = V_{cc}$

by joining these points, a straight line is drawn. the resulting line on graph is called load line.

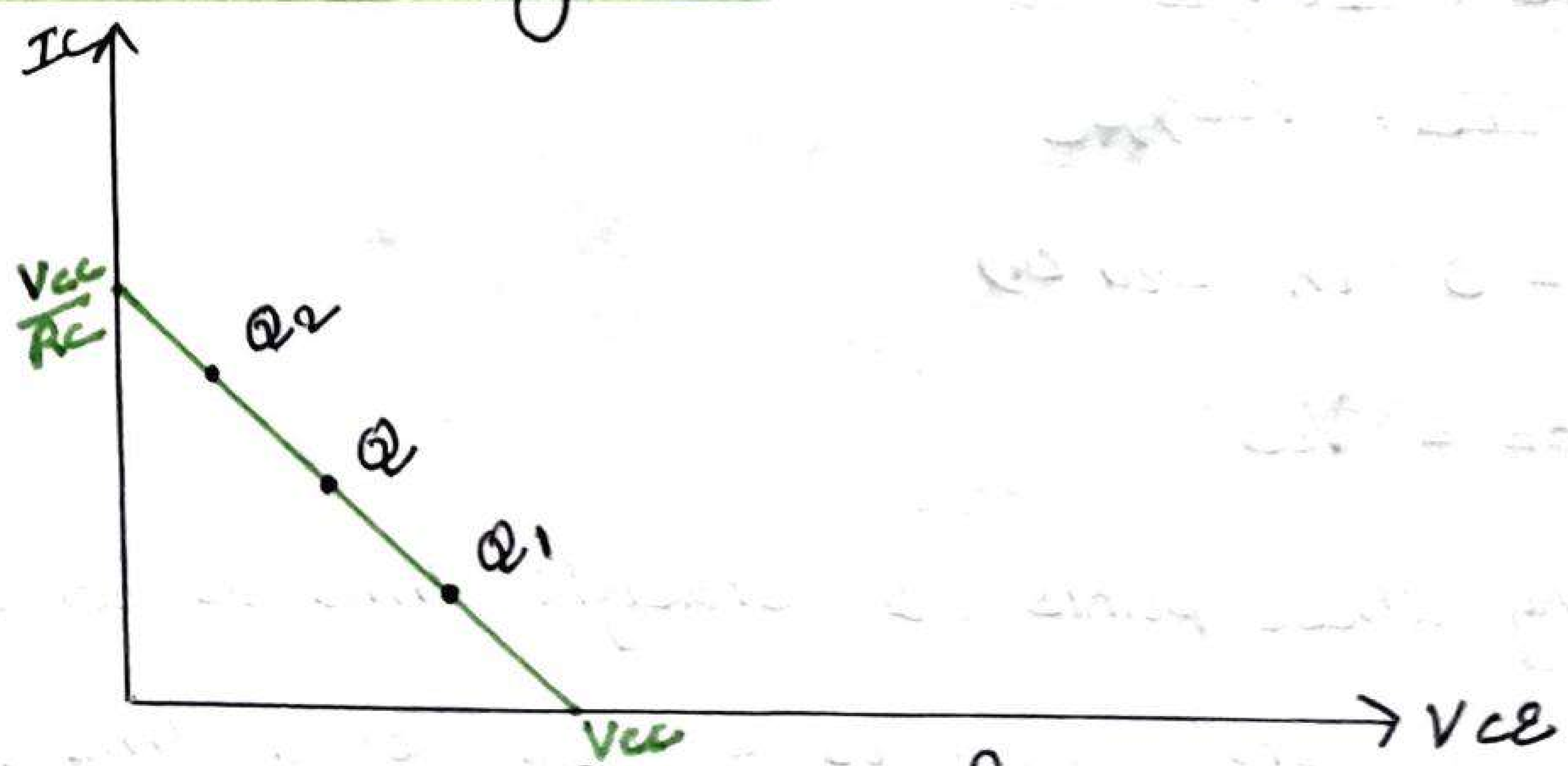


Operating Point or Q-point

Q-point is called quiescent point or operating point. It specifies the collector current Ic & Vce that exist when no i/p signal is applied.

It is also called operating point because the variation in Vce & Ic takes place about this point when the signal is applied. The best position for this point is the midway b/w the cut off & saturation point where $V_{ce} = \frac{1}{2} V_{cc}$.

Selection of Operating Point

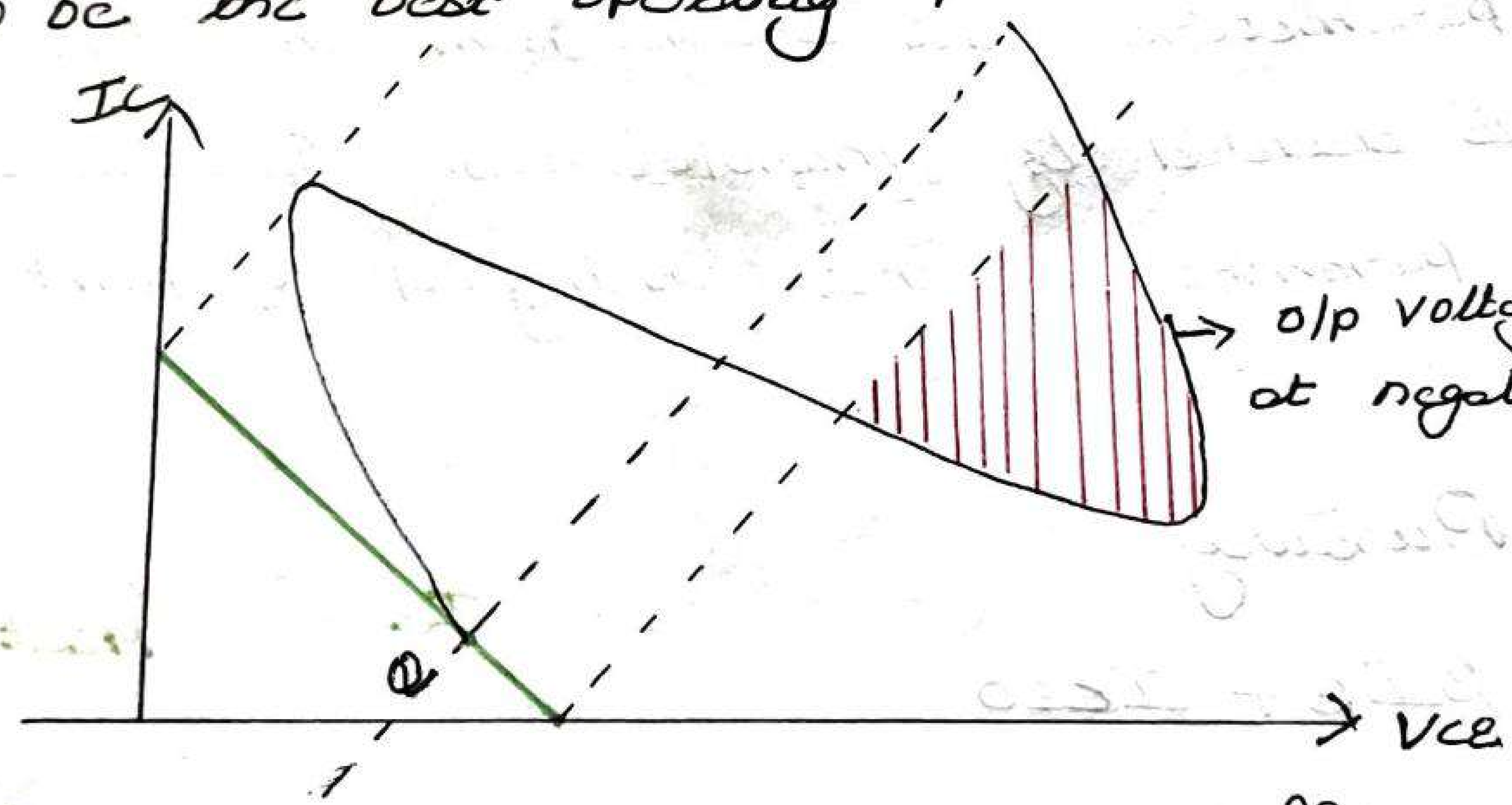


For the proper amplification of i/p signal, the selection of operating point is important.

At the point Q_1, it is nearer to cut-off region, the o/p current & voltage would be allowed to vary but it will clipped at the negative peak of the i/p signal.

At the point Q_2, it is nearer to saturation region, the o/p signal would be clipped at positive peak of i/p signal.

The point 'Q' located at the centre of load line seen to be the best operating point.



Q-point nearer to cut-off region.

We have to fix operating point at a particular point. This process is called biasing.

During amplification, operating point is shifting because, the reasons are given below.

Need for bias stabilization

1) The transistor parameters are temp. dependent

i/p imp, o/p imp, current gain, voltage gain are the four transistor parameters. When temp. varies above parameters are changed. So proper amplification does not takes place.

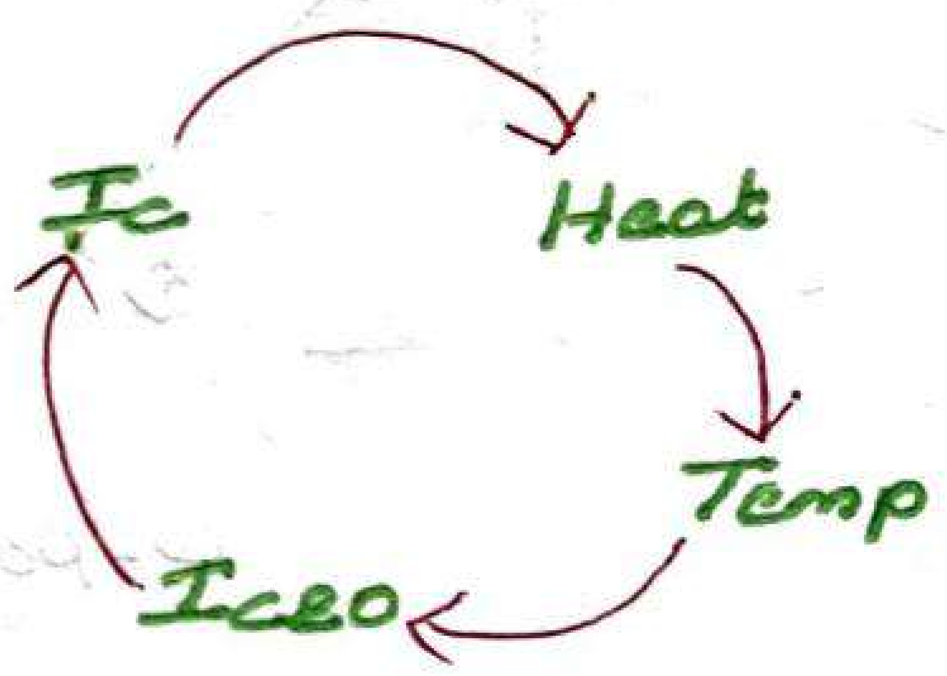
2) Transistor parameter 'β' will change from unit to unit.

The parameters will change from one transistor to other. It is decided by manufacturer. Because of this change in parameters, the shifting of Q-point occurs.

3) Thermal Runaway.

$I_C = \beta I_B + I_{CEO}$

$I_{CEO} \Rightarrow$ leakage current.



Consider a C.E configuration. It is a phenomenon in C.E configuration. During amplification Ic increases, heat increases, temp. increases covalent bonds are broken & more electrons are produced, Iceo increase & again Ic increase, it will repeat. This is a cumulative process. It continues until transistor burn away. This is called thermal run away

R_1 & R_2 ⇒ used for biasing & stabilization ckts

R_E ⇒ Emitter bypass

C_C ⇒ Coupling capacitors.

Potential divider biasing is used in ckt because it provides good stabilization of the operating point.

C_{in} ⇒ i/p capacitor of about 10µf is used to couple the signal to the base of txr. It allows only ac signal to flow. In the absence of C_{in}, the signal source resistance will come across R_2 & this changes the bias.

C_E ⇒ Emitter bypass capacitor (100µf) is used to provide a low reluctance path. In the absence of this capacitor, amplified ac signals flowing through R_E, will cause voltage drop across it which inturn will feedback the i/p side & reduce the o/p voltage.

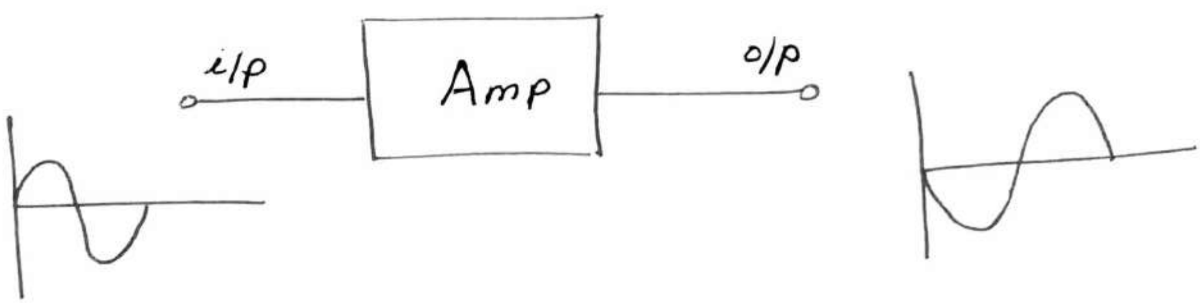
C_C ⇒ Coupling capacitor or blocking capacitor (10µf). It blocks dc component of o/p signal. In the absence of C_C, the resistor R_C will come in parallel to R_1 of second stage, thereby changing the biasing condition of next stage.

Amplifying Action

When a signal is applied b/w the base & the emitter terminals of a properly biased transistor, a small base current starts flowing. Because of transistor action, a much larger ac current (β times base current) flows through the R_C. Since the value of collector resistance is high, larger voltage appears across R_C.

PHASE REVERSAL

There is 180° phase diff b/w i/p & o/p



o/p $V_{CE} = V_{CC} - i_C R_C$

With increase in signal voltage in the positive half cycle, the base current increases causing increase in the collector current, so the drop across R_C i.e. $i_C R_C$ increases. So the o/p voltage decreases. So the signal voltage increases in positive direction, the o/p voltage increases in negative direction.

Load Line Analysis

The relationship b/w the collector-emitter o/p voltage & the collector current I_C is linear.

Apply KVL to o/p side of amplifier.

$$V_{CC} = I_C R_C + V_{CE} + I_C R_E \quad \text{--- (1)}$$

$$V_{CC} = V_{CE} + I_C (R_C + R_E)$$

$$\because I_E \approx I_C$$

$$I_C (R_C + R_E) = V_{CC} - V_{CE}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

During cut off, $I_C = I_E = 0$, substitute it in equ (1)

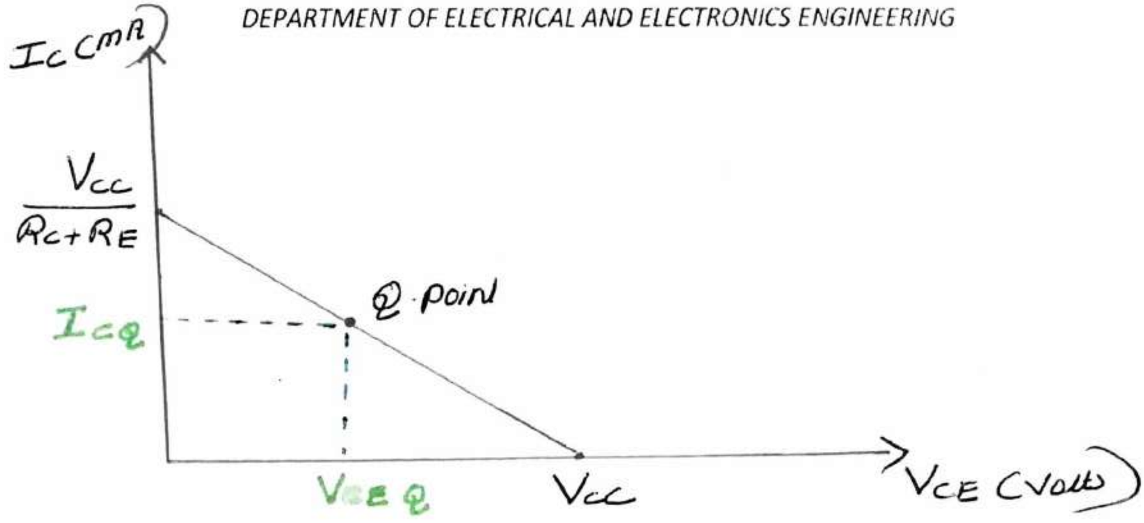
$$\underline{\underline{V_{CC} = V_{CE}}}$$

During saturation $V_{CE} \approx 0$, sub. it in equ (1)

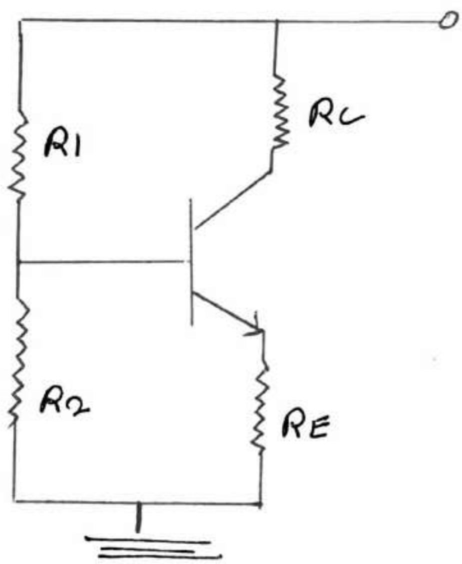
$$V_{CC} = I_C R_C + I_E R_E$$

$$= I_C (R_C + R_E)$$

$$\underline{\underline{I_C = \frac{V_{CC}}{R_C + R_E}}}$$



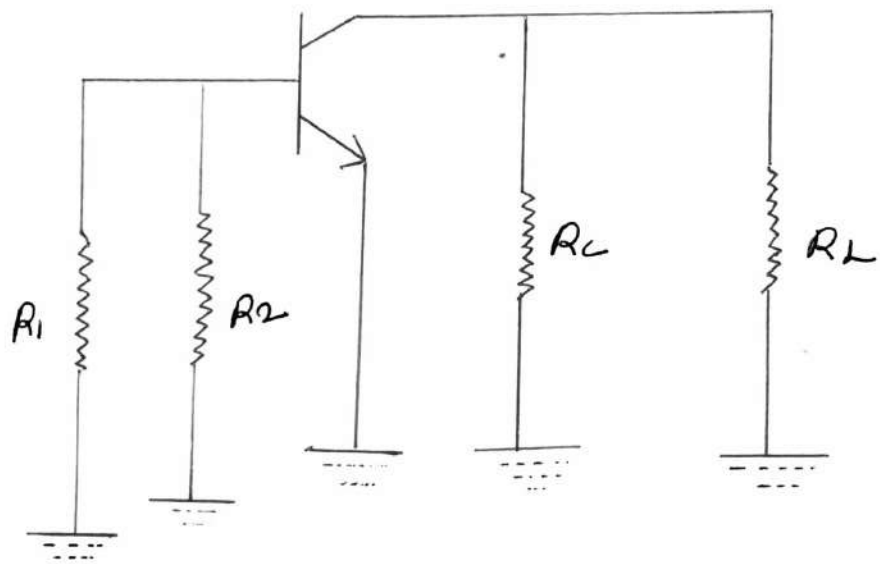
DC Equivalent Circuit



It can be drawn by reducing all the ac sources to zero & opening all the capacitors because the capacitors do not allow the flow of the DC current & act as open.

AC Equivalent Circuit

If AC is applied, dc supplies need not be considered. AC equivalent circuit can be drawn by reducing all the dc sources to zero & short circuiting all capacitors.



The ckt explains the behaviour when viewed in the ac conditions. The collector resistance R_c comes in parallel with R_L.

10 a) A transistor used in CE connection has the following set of h parameters when the d.c. operating point is V_{CE} =5V and I_C = 1 mA; h_{ie} =1700 Ω ; h_{re} =1.3 ×10-4; h_{fe} = 38; h_{oe} = 6×10^{-6} ℧. If the a.c. load r_L seen by the transistor is 2 KΩ , find (i) the input impedance (ii) current gain (iii) voltage gain (5)

10 (a) $Z_{in} = h_{ie} - \frac{h_{re} h_{fe}}{h_{oe} + \frac{1}{Z_L}}$.

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i) $Z_{in} = 1700 - \frac{1.3\times10^{-4}\times 38}{6\times10^{-6}+\frac{1}{2000}} = \underline{\underline{1690\,\Omega}}$ — (2)

ii) Current gain $A_i = \frac{h_{fe}}{1+h_{oe}R_L} = \frac{38}{1+6\times10^{-6}\times2000}$

$= 37.6$ —— (2)

iii) Voltage gain $A_V = \frac{-h_{fe}}{Z_{in}\left[h_{oe}+\frac{1}{R_L}\right]}$

$= \frac{-38}{1690\left(6\times10^{-6}+\frac{1}{2000}\right)} = \underline{\underline{-44.4}}$ —— (1)

b) * Width of depletion layer controlled by gate-to source Voltage.

* Effective cross section decreased with increasing reverse bias. I_D is a function of V_{GS}.

* FET Voltage controlled device, do not need biasing current. By applying reverse bias voltage to gate terminal, channel is pinched, so that current is switched off completely

(2.5)

Drain resistance r_d.

Transconductance, g_m

Amplification factor, μ.

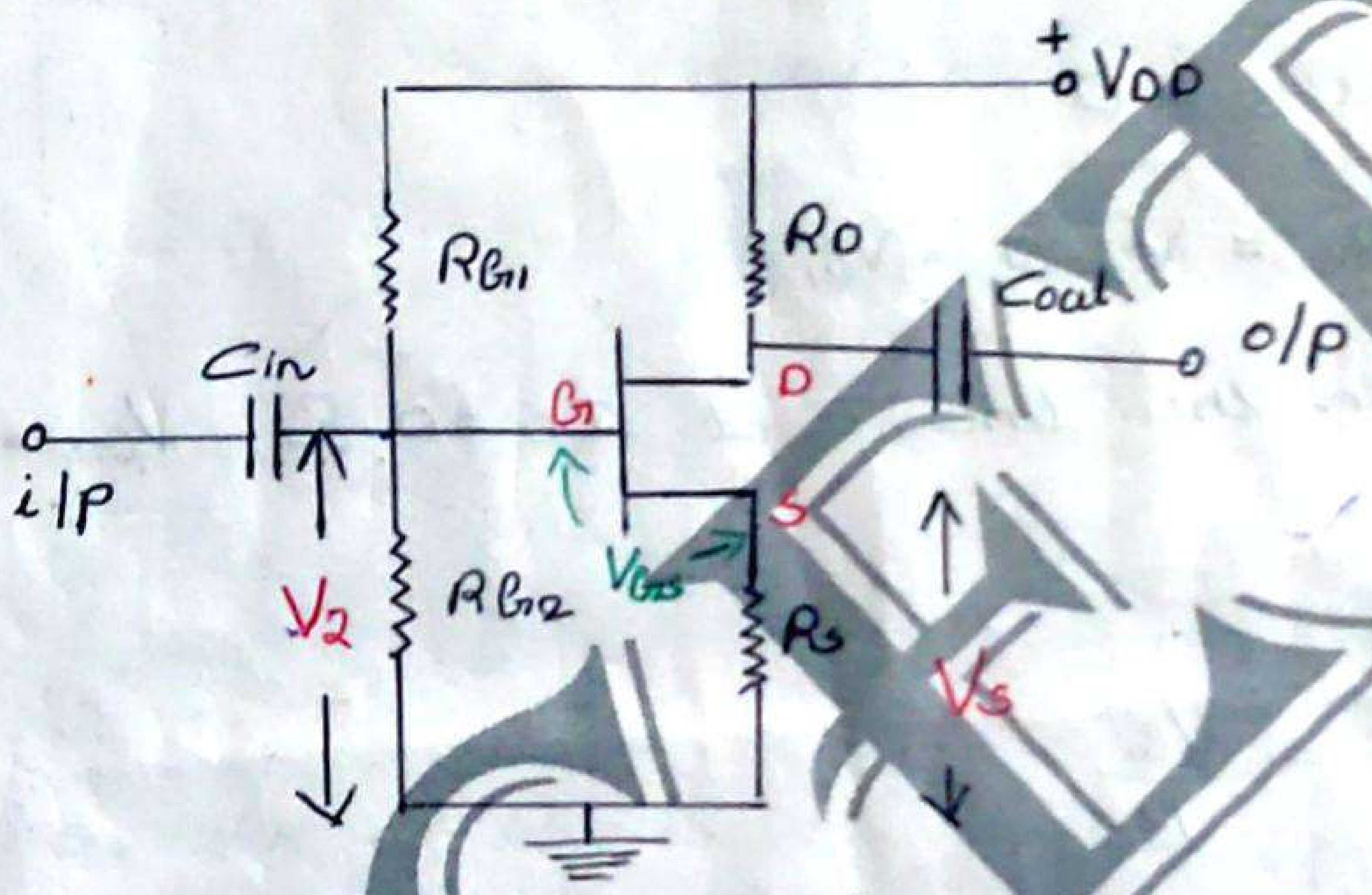
Write down expressions also.

(2.5)

FET Biasing

Unlike the BJT the thermal runaway doesn't occur with FET's.

Potential Divider biasing of FET



The resistors R_{G1} & R_{G2} provides a potential divider across the drain supply V_{DD}. The voltage across R_{G2} provides the necessary bias.

$$\text{Gate Voltage } V_G = V_{DD} \times \frac{R_{G2}}{R_{G1}+R_{G2}}$$

& $V_{GS} = V_G - V_S$, where $V_S = I_S R_S = I_D R_S$

$$V_{GS} = V_G - I_D R_S .$$

The ckt is so designed that $I_D R_S$ is larger than V_G so the V_{GS} is negative. This provides a negative gate voltage.

$$V_2 = V_{GS} + I_D R_S$$

$$I_D = \frac{V_2 - V_{GS}}{R_S}$$

then $V_{DS} = V_{DD} - I_D (R_D + R_S)$

The value of I_D & V_{DS} determines the operating
In Voltage divider biasing either $I_D = 0$, $V_{GS} \neq 0$

For $I_D = 0$

$$V_S = I_D R_S = 0 \times R_S = 0$$

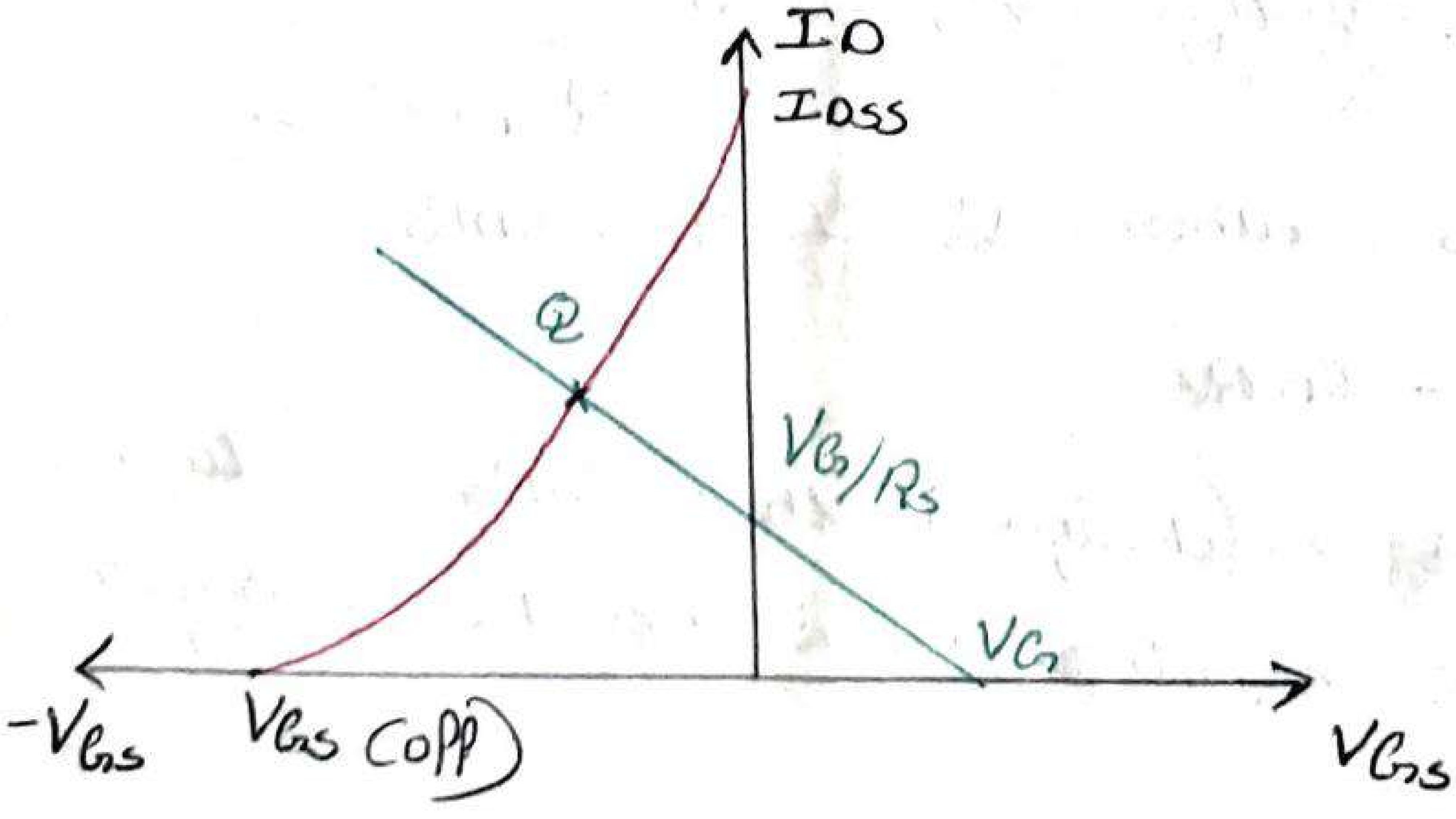
$$V_{GS} = V_G - I_D R_S = V_G - 0 = V_G$$

$\therefore$ One point on the line is at $I_D = 0$ & $V_{GS} = V_G$

For $V_{GS} = 0$

$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{V_G}{R_S}$$

The second point on the line is at $I_D = \frac{V_G}{R_S}$ & $V_{GS} = 0$. The point at which the load line intersects the transistor characteristic curve is Q point.

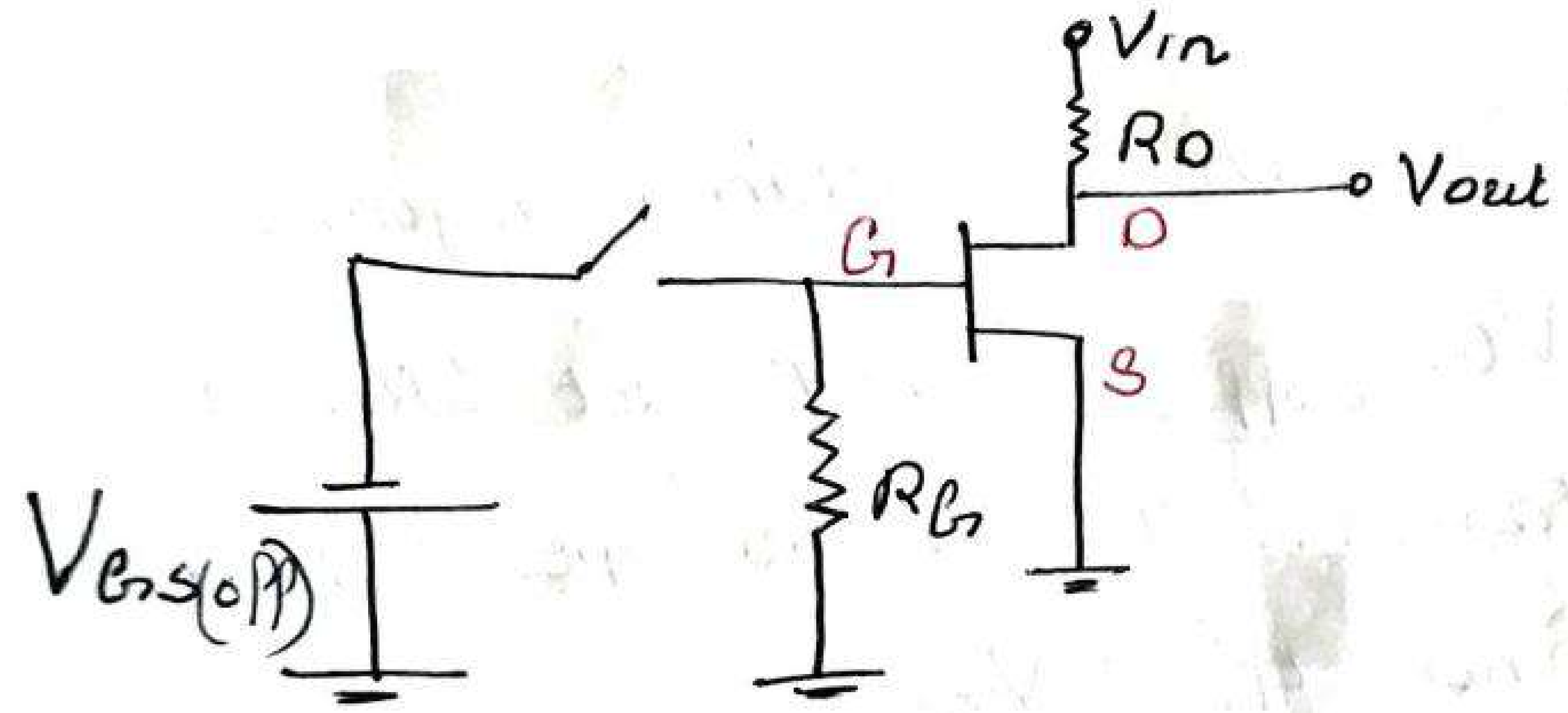


ET as a switch

V_{in} = i/p voltage

Either no gate voltage is applied to FET, $V_{GS} = 0$, FET becomes saturated & it behaves like a small resistance.

then o/p = $V_{out} = \dfrac{V_{in} \times R_{DS}}{R_{DS(on)} + R_D}$

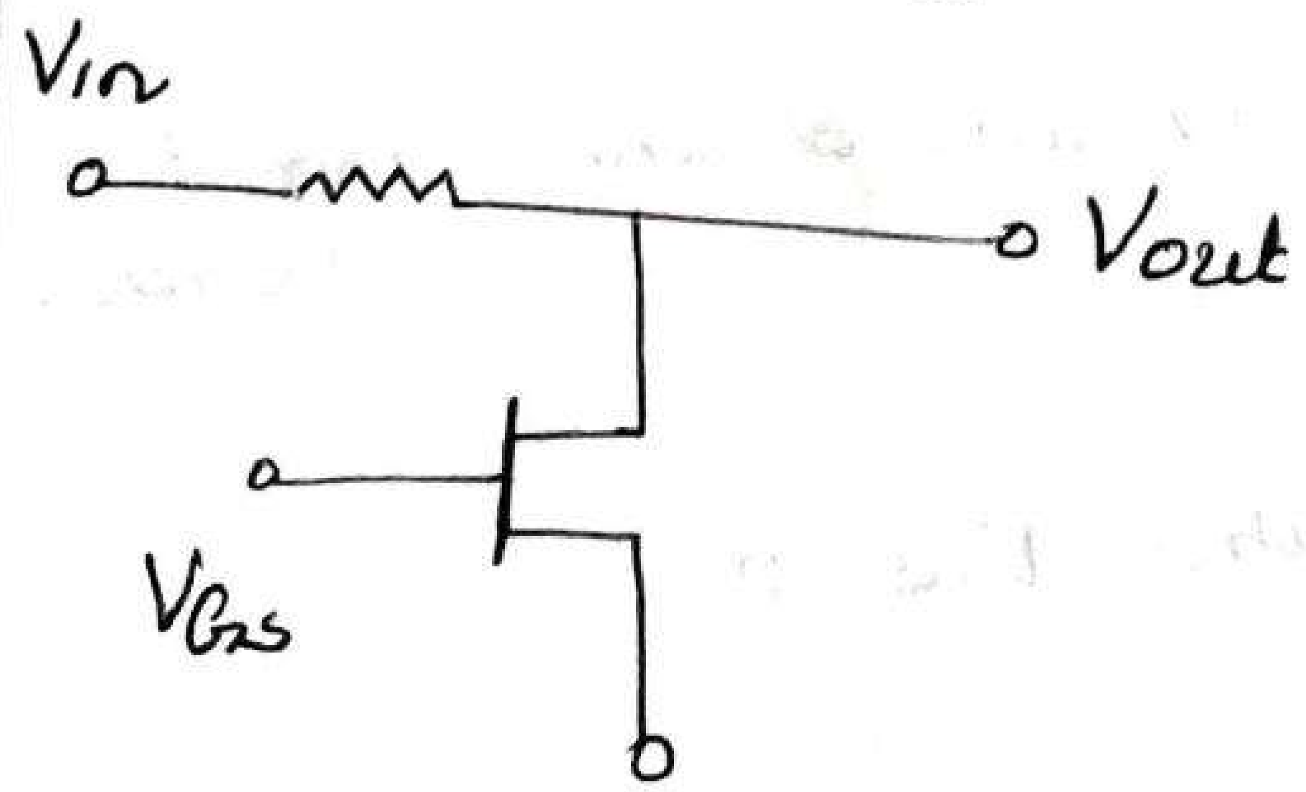


∴ the value of RD is very large, the o/p $V_{out} = 0$

Either a negative voltage $V_{GS(off)}$ is applied, the FET operates in the cut off region, it act as very high resistance, hence the o/p nearly equal to i/p

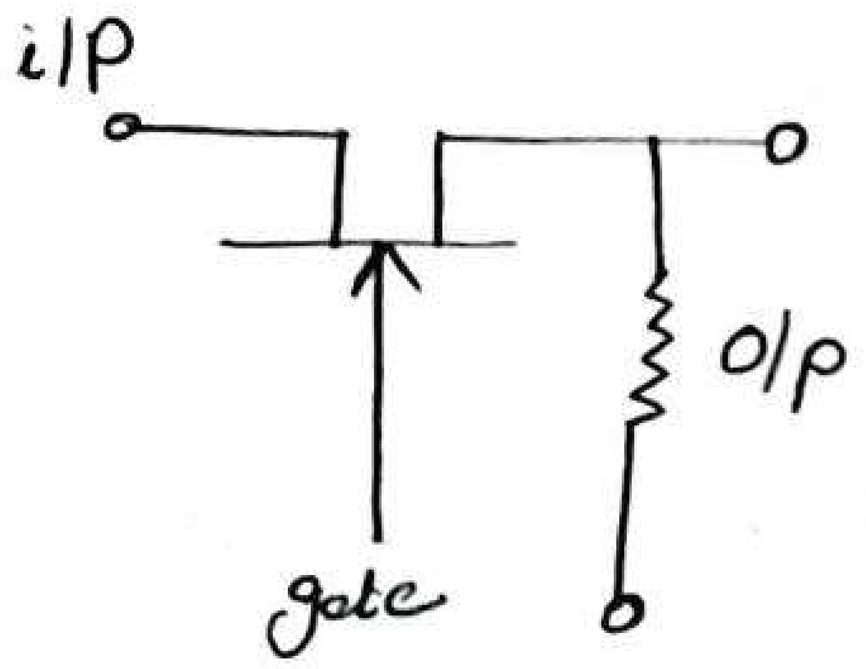
$$V_{out} = \frac{R_{DS}}{R_D + R_{DS(off)}} V_{in}$$

$R_{DS(off)} \gg R_D$, so $V_{out} \approx V_{in}$



$\Rightarrow$ $V_{GS} = 0 \Rightarrow V_{out} = 0$
(high)
V_{GS} (low, -ve) $\Rightarrow V_{out} = V_{in}$

Short Switch



$V_{GS} = 0$ (high) $\Rightarrow$ $V_{out} = V_{in}$

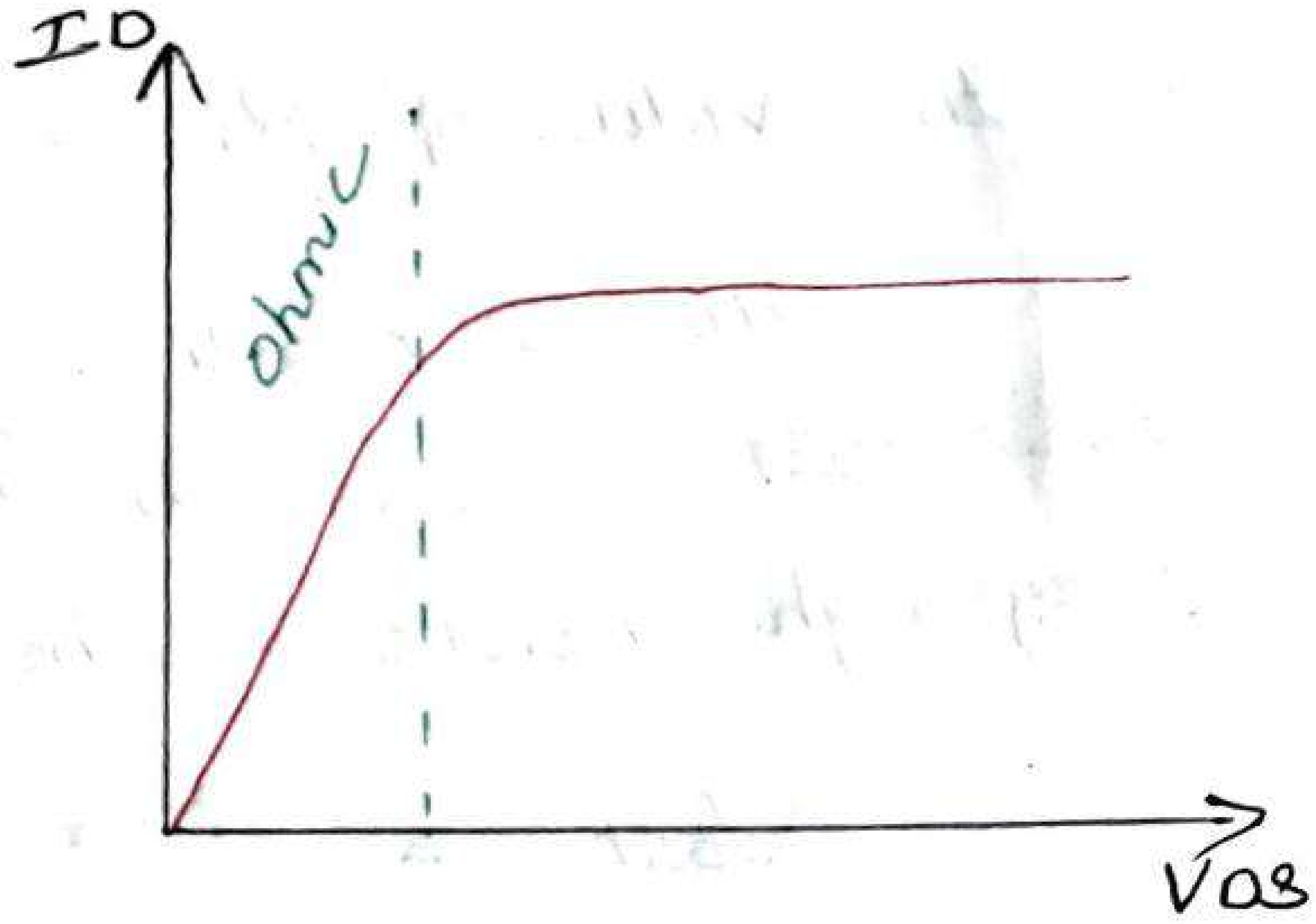
$\Rightarrow$ V_{GS} (low) $\Rightarrow$ $V_{out} = 0$

Series Switch

FET as Voltage Controlled Resistance

When JFET operates in the ohmic region with V_{GS} b/w 0 & $V_{GS(off)}$, JFET act like a voltage controlled resistance. It can be operated in the region prior to pinch off (V_P).

In this region drain to source resistance can be controlled by V_{GS}.



$$r_{ds} = \frac{V_{DS}}{I_D}$$

r_{ds} depends on the value of V_{GS}.

$V_{GS} = 0$, r_{ds} is minimum

V_{GS} = more negative, r_{ds} increases

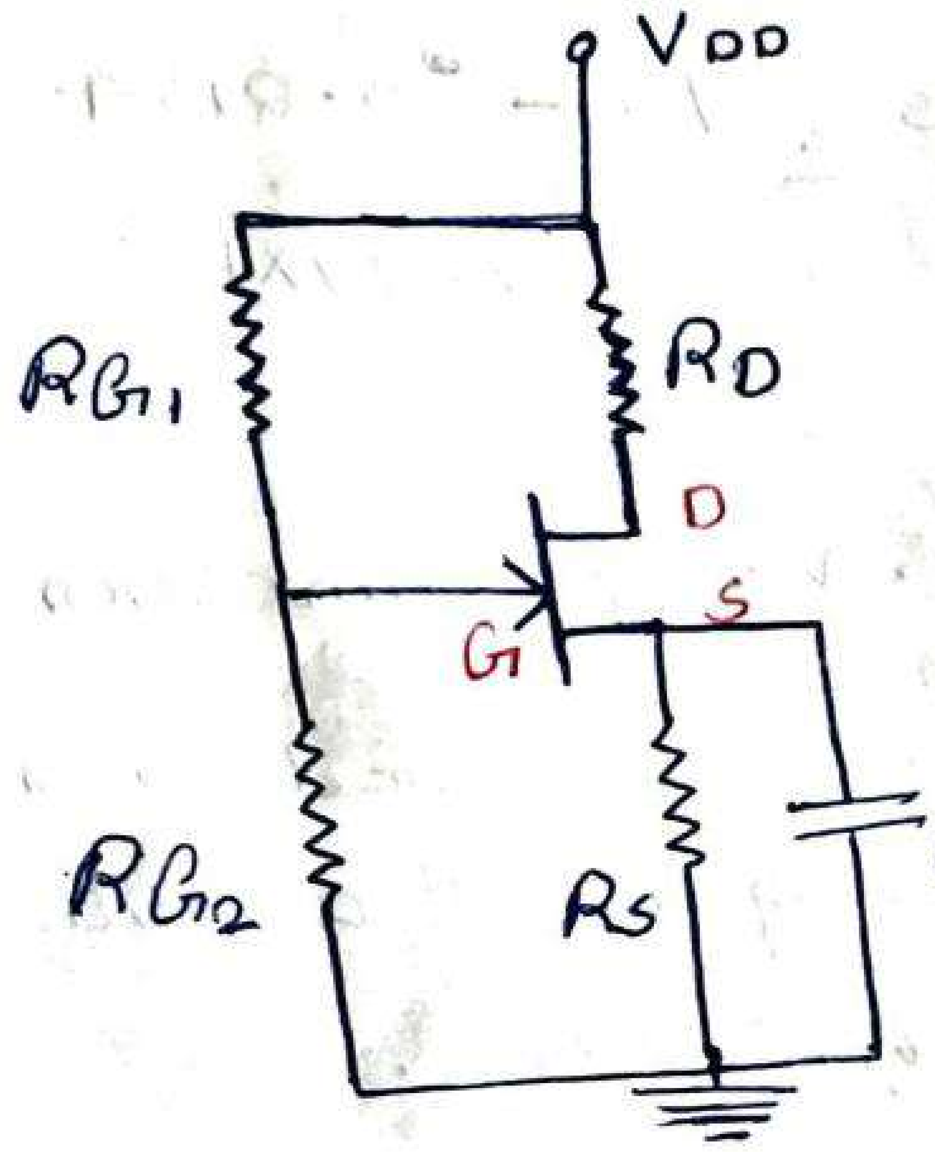
When V_{GS} becomes negative, I_D or the drain current reduces.

$$r_{ds} = \frac{\overset{(const)}{100\,mV}}{0.8\,mA} = 125\,\Omega \quad \text{when } V_{GS} = 0$$

$r_{ds} = \dfrac{100\,mV}{0.4\,mA} = 250\,\Omega$ when $V_{GS} = -2V$.

So JFET act as the VCR in ohmic region

Q) A JFET amplifier with stabilized biasing ckt is shown. $V_P = -2V$, $I_{DSS} = 5mA$, $R_L = 910\Omega$, $R_S = 2.29\,k\Omega$, $R_{G_1} = 12\,M\Omega$, $R_{G_2} = 8.57\,M\Omega$ & $V_{DD} = 24\,V$. Find the value of drain current I_D



$V_{DD} = 24\,V$.

$R_L = 910\,\Omega$

$R_S = 2.29\,k\Omega$

$I_{DSS} = 5mA$

$V_P = -2V$

$R_{G_1} = 12\,M\Omega$

$R_{G_2} = 8.57\,M\Omega$

$\{ V_G = V_{GS} + I_D$

$$V_G = \frac{V_{DD} \times R_{G_2}}{R_{G_1} + R_{G_2}} = \frac{24 \times 8.57}{8.57 + 12} = \underline{\underline{10V}}$$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 = 5 \times 10^{-3}\left[1 - \left(\frac{V_G - I_D R_S}{-2}\right)\right]$$

$$I_D = 5 \times 10^{-3}\left[1 - \left(\frac{10 - I_D \times 2.29 \times 10^{3}}{-2}\right)\right] \quad -(1)$$

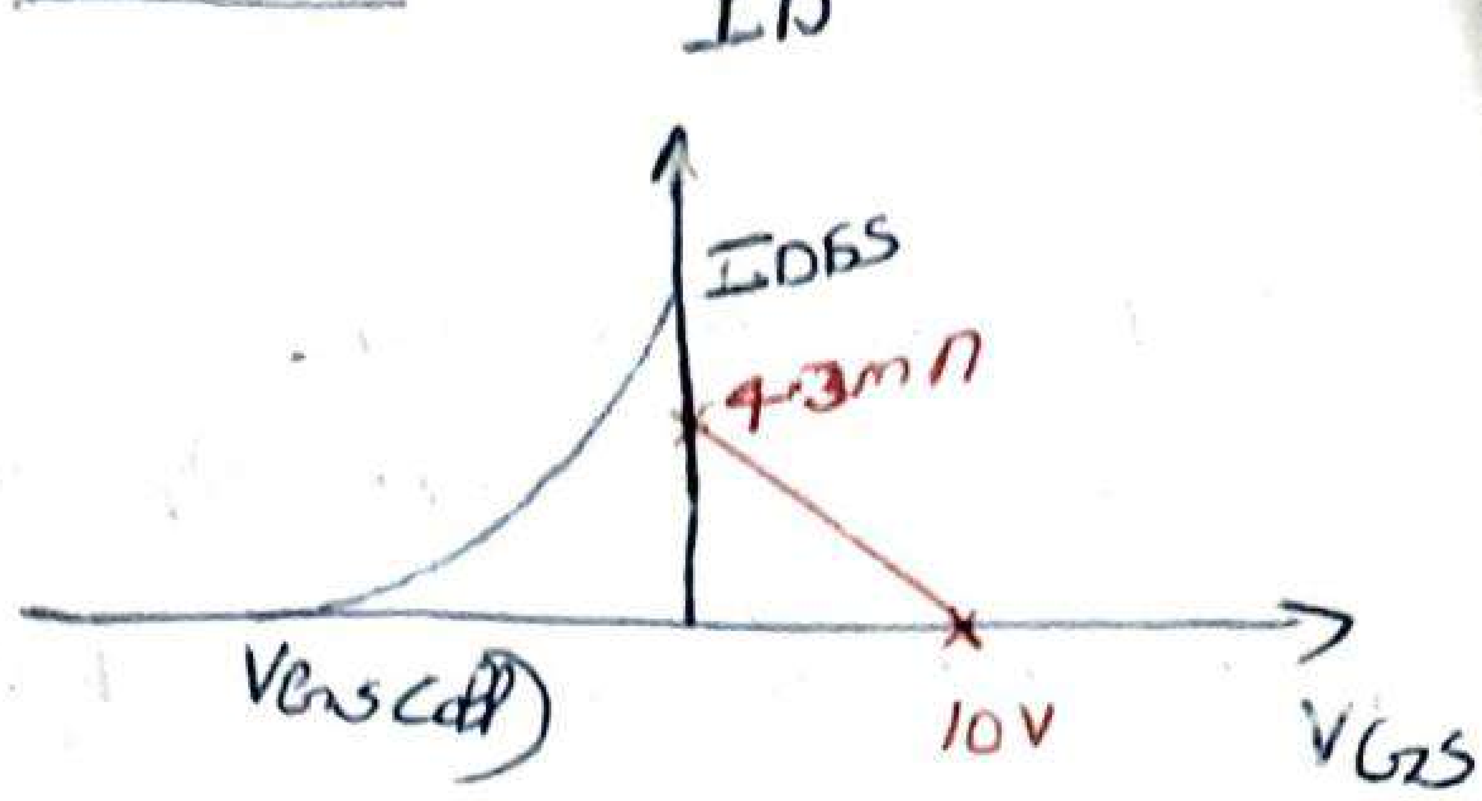
solving (1)

$I_D = \underline{\underline{4.46\,mA}}$

Load line pts

$V_{GS} = V_G$

$= \underline{10V}$



$$I_D = \frac{V_G}{R} = \frac{10}{2.29 \times 10^3} = \underline{4.3}\ mA$$

Q.) The gm of FET voltage amplifier ckt is 2500 microsiemens & load resistance is 12 kΩ. Determine voltage gain of amplifier ckt. Assume rd & $R_D \gg R_L$.

$g_m = 2500 \times 10^{-6} S$

$R_L = 12 \times 10^3$

$$A_V = \frac{V_{out}}{V_{in}} = \frac{I_d (r_d \parallel R_D \parallel R_L)}{V_{in}}$$

$$= \frac{-g_m V_{in} (r_d \parallel R_D \parallel R_L)}{V_{in}}$$

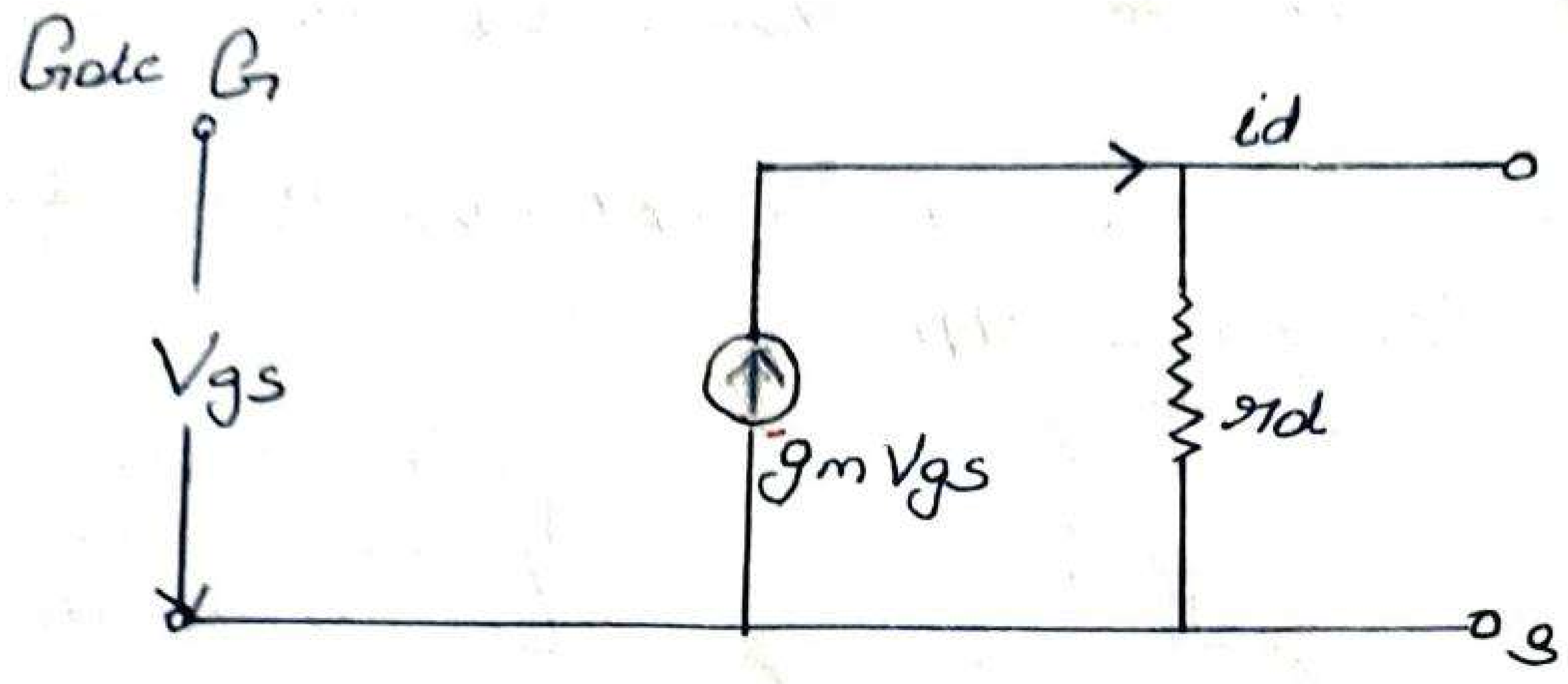
$$= -g_m (r_d \parallel R_D \parallel R_L)$$

$r_d \,\&\, R_D \gg R_L$

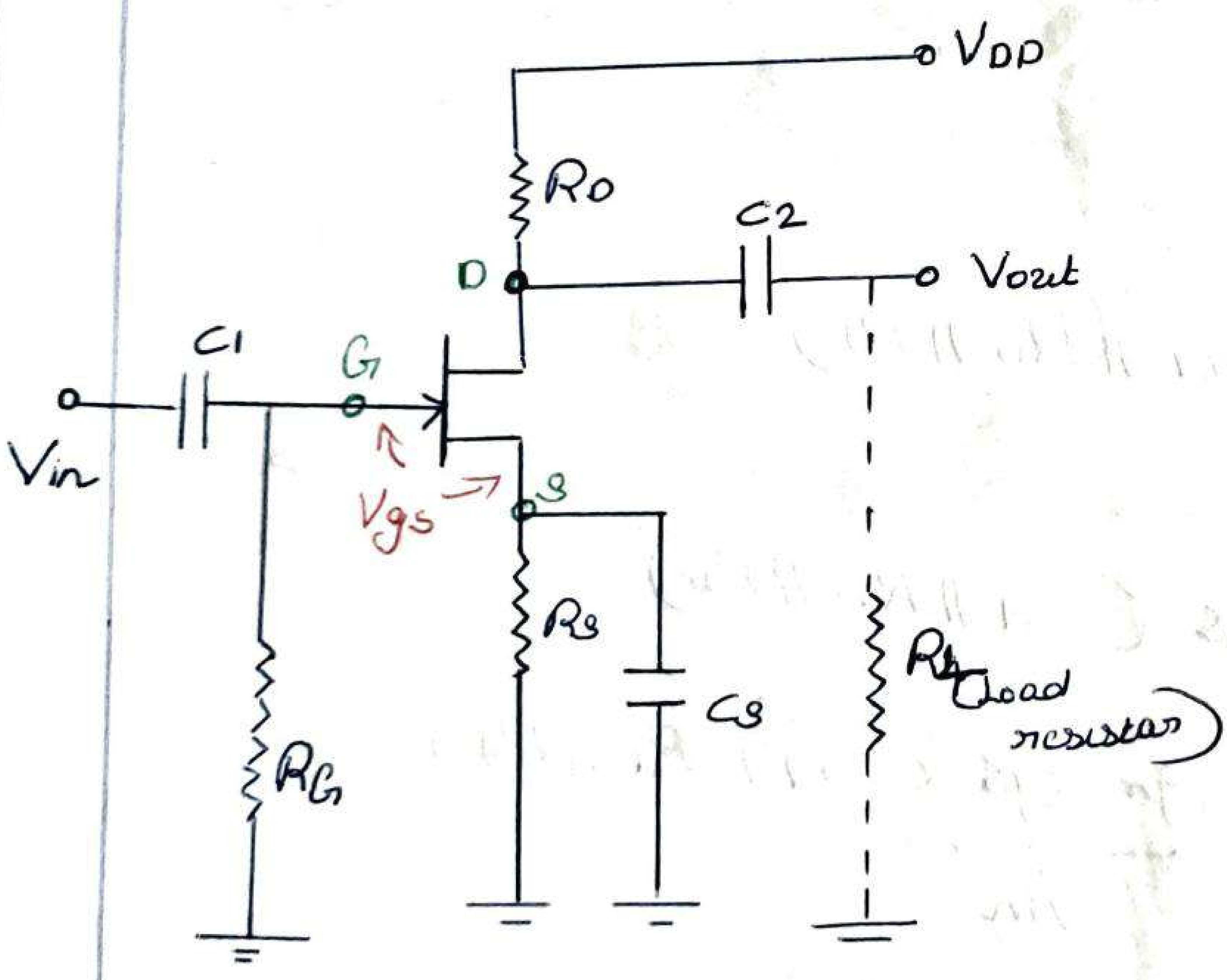
$$A_V = -g_m R_L = -2500 \times 10^{-6} \times 12 \times 10^3$$

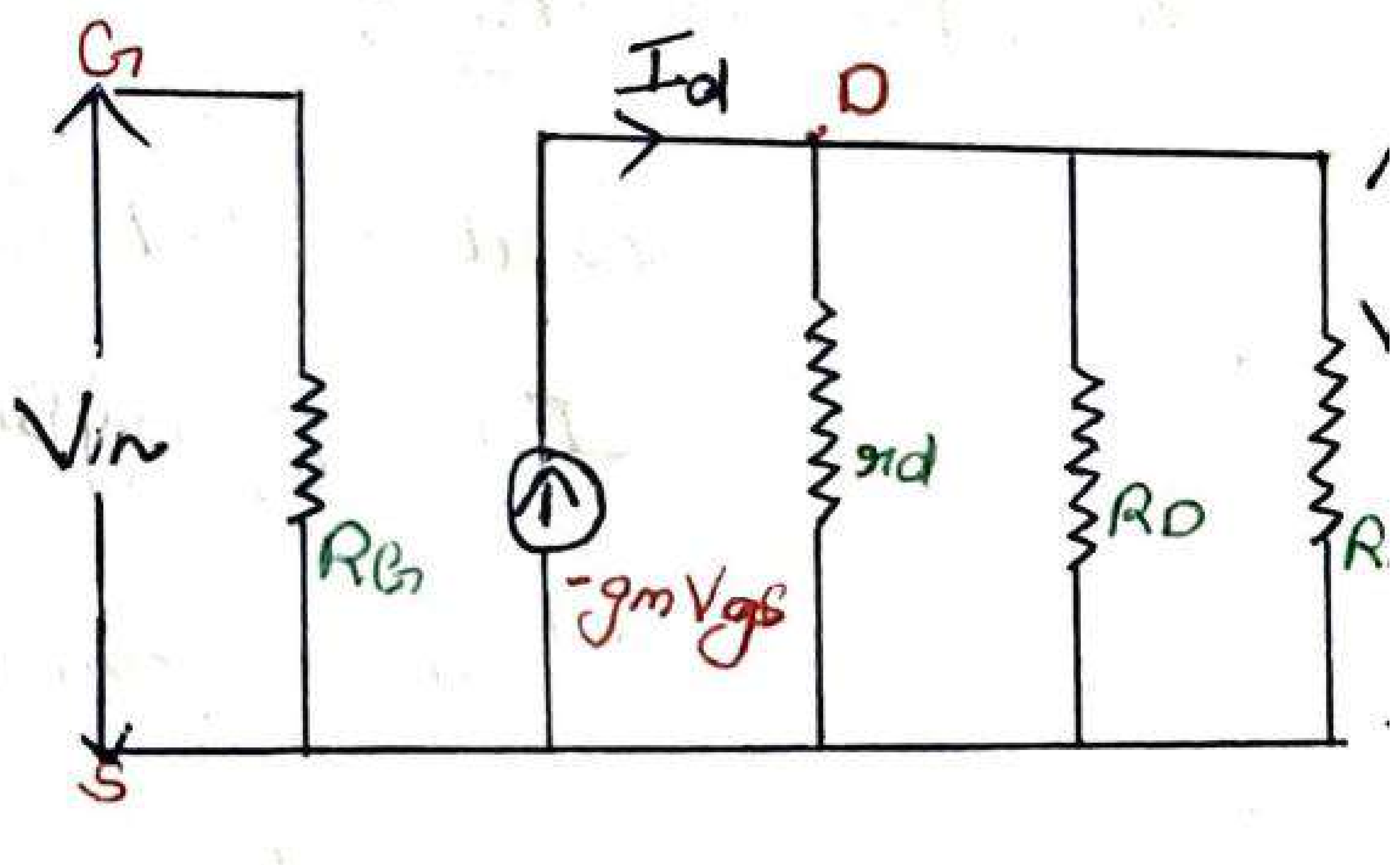
$$= \underline{-30}$$

FET small signal model (Low Frequency)



Common Source JFET amplifier





AC Equivalent Ckt

C_1 & C_2 ⇒ coupling capacitor

C_S ⇒ bypass capacitor

V_{in} ⇒ i/p voltage

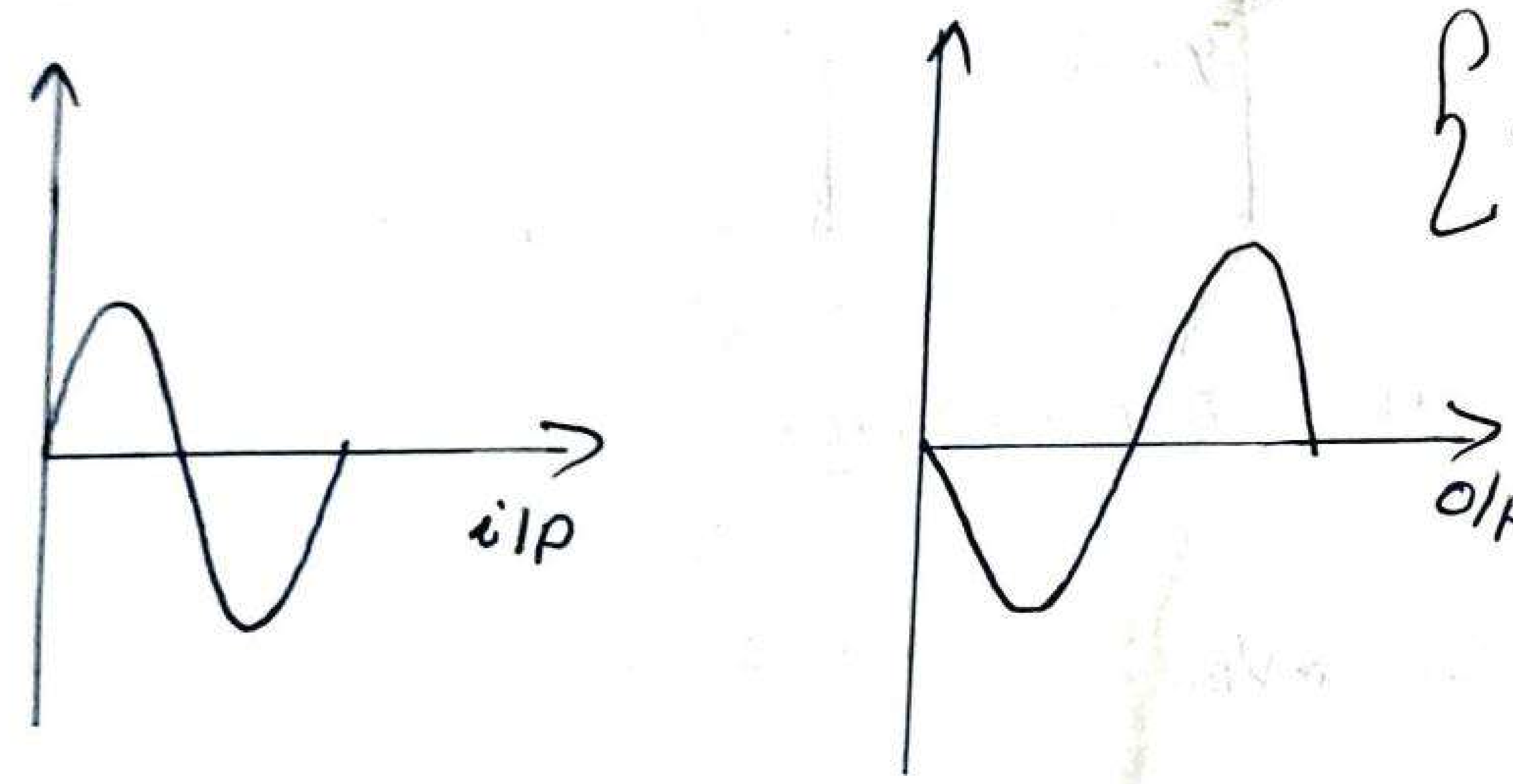
V_{out} ⇒ o/p voltage $= V_D$

$V_D = V_{DD} - I_D R_D$

⇒ During +ve half cycle of i/p, V_{gs} increases
∴ I_D also increases. Hence V_D decreases

⇒ During -ve half cycle of i/p, V_{gs} decreases
∴ I_D also decreases. Hence V_D increases.

In common - Source JFET amplifier, there exist a phase shift of 180° b/w i/p & o/p



{ For drawing ac-equivalent ckt
1) gnd all DC source
2) S.C the capacitance
3) R_G, r_d, R_D, R_L are grounded }.

Voltage Gain :

$$V_{out} = I_d (r_d \parallel R_D \parallel R_L)$$

$V_{gs} \approx V_{in}$

$$I_d = -g_m V_{gs}$$

$$V_{out} = -g_m V_{gs} (r_d \parallel R_D \parallel R_L)$$

$$A_V = \frac{V_{out}}{V_{in}} = \frac{-g_m V_{gs} (r_d \parallel R_D \parallel R_L)}{V_{in}}$$

$$A_V = -g_m (r_d \parallel R_D \parallel R_L)$$

Usually $r_d >> R_D$ & R_L

$$\therefore A_V = -g_m (R_D \parallel R_L)$$

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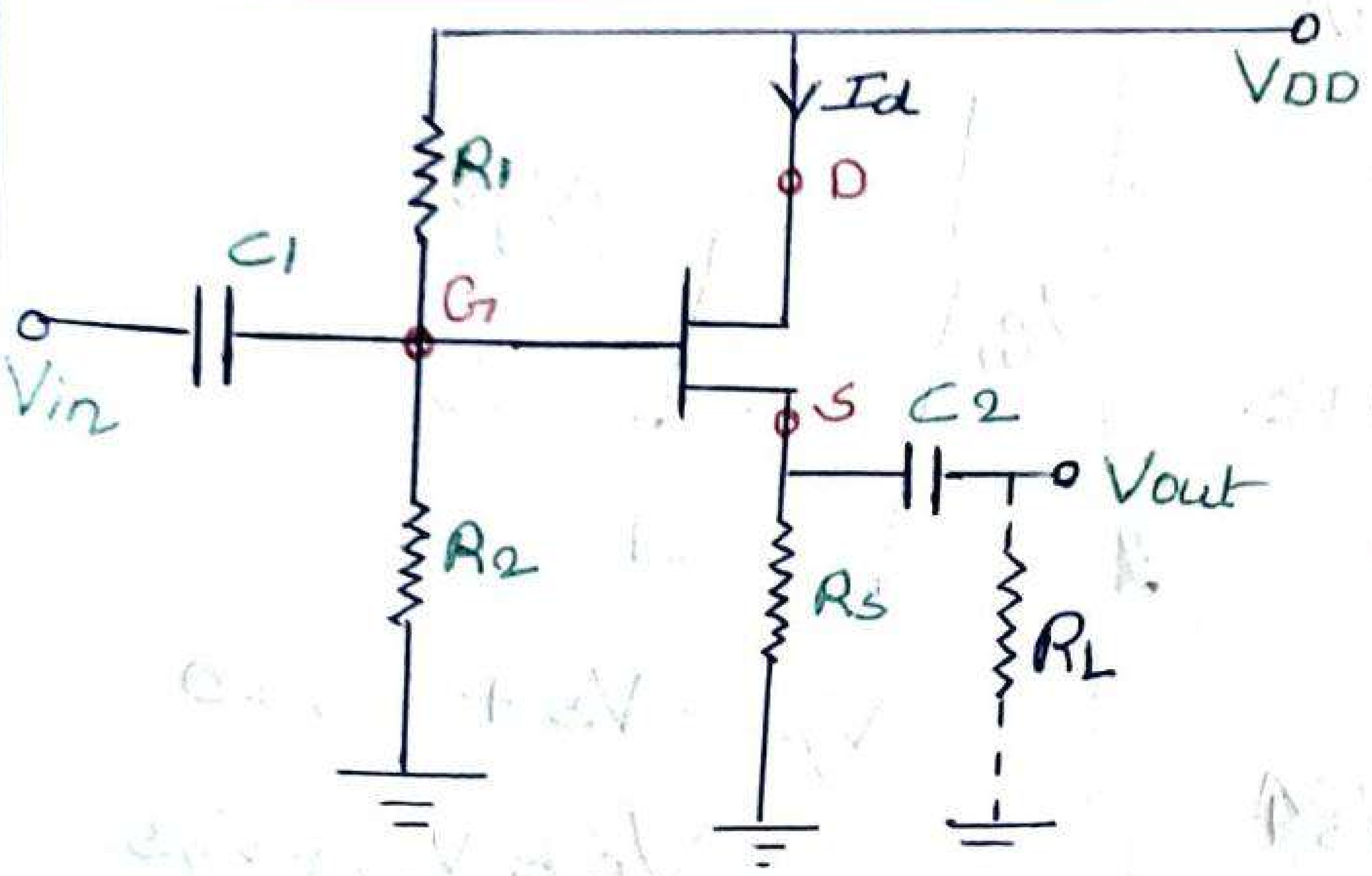
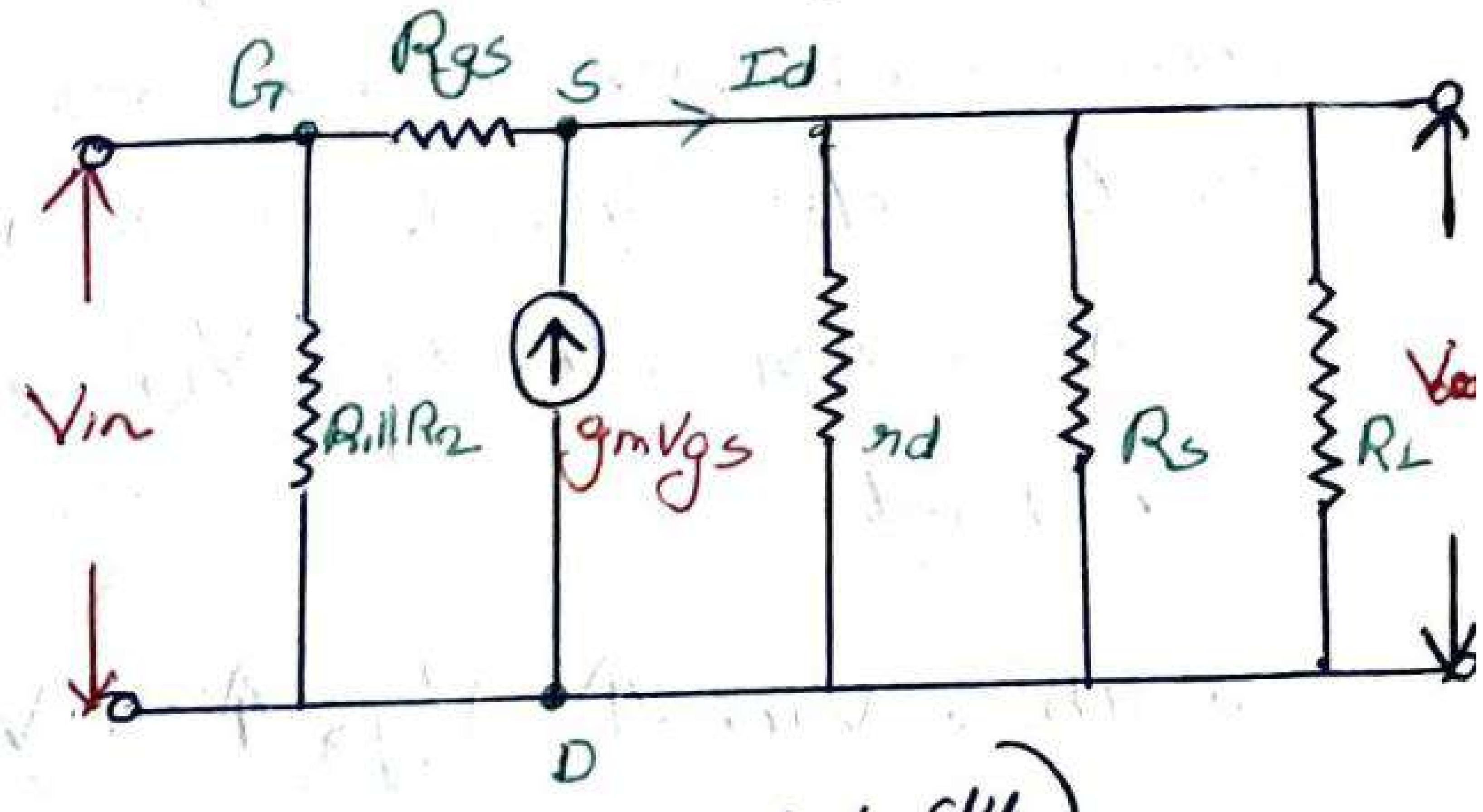
Common Drain JFET Amplifier





(AC equivalent ckt)

$C_1, C_2 \Rightarrow$ Coupling capacitor

$R_1, R_2 \Rightarrow$ biasing resistors (potential divider)

No bypass capacitors are used.

$V_s \Rightarrow$ o/p voltage

$V_s = V_G + V_{gs}$

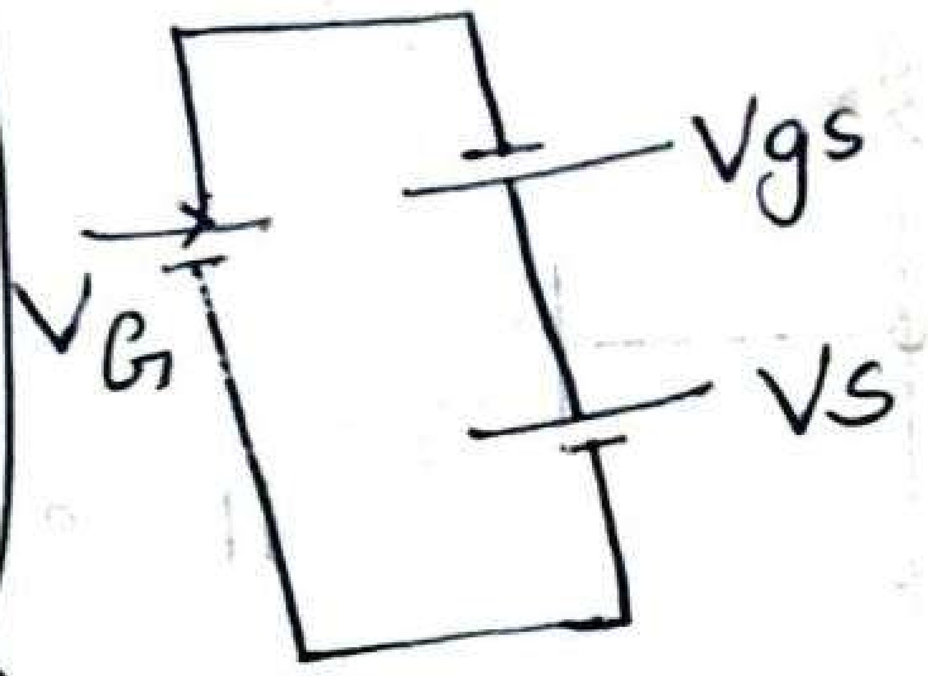
$\Rightarrow$ During +ve half cycle of i/p, V_s is high

$\Rightarrow$ During -ve half cycle of i/p, V_s is low

* Because the o/p voltage at FET source terminal follows variations in signal voltage applied to gate, the common drain ckt is also called Source follower

Explanation

The source voltage
$V_s = V_G + V_{gs}$ when
a signal is applied to FET
gate through C_1, V_{gs}
increases or decreases
as the i/p signal goes +ve
& -ve respectively. V_G is
constant.



$$V_{gs} - V_s + V_G = 0$$
$$V_s = V_G + V_{gs}$$

⇒ when $V_{in} \uparrow$ $V_{gs} \uparrow$ & $V_s \uparrow$
⇒ when $V_{in} \downarrow$ $V_{gs} \downarrow$ & $V_s \downarrow$

V_s is the output voltage.

The o/p voltage V_s follows the i/p, ∴ it is called
source follower.

$$A_V = \text{Voltage gain} = \frac{V_{out}}{V_{in}}$$

$$V_{out} = I_d (r_d \| R_s \| R_L) = g_m V_{gs} (r_d \| R_s \| R_L)$$
$$V_{in} = V_{gs} + V_{out} = V_{gs} + g_m V_{gs} (r_d \| R_s \| R_L)$$
$$= V_{gs} (1 + g_m (r_d \| R_s \| R_L))$$

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_m \cancel{V_{gs}} (r_d \| R_s \| R_L)}{\cancel{V_{gs}} (1 + g_m (r_d \| R_s \| R_L))} = \frac{g_m (r_d \| R_s \| R_L)}{1 + g_m (r_d \| R_s \| R_L)}$$

usually $r_d \gg R_s \| R_L$

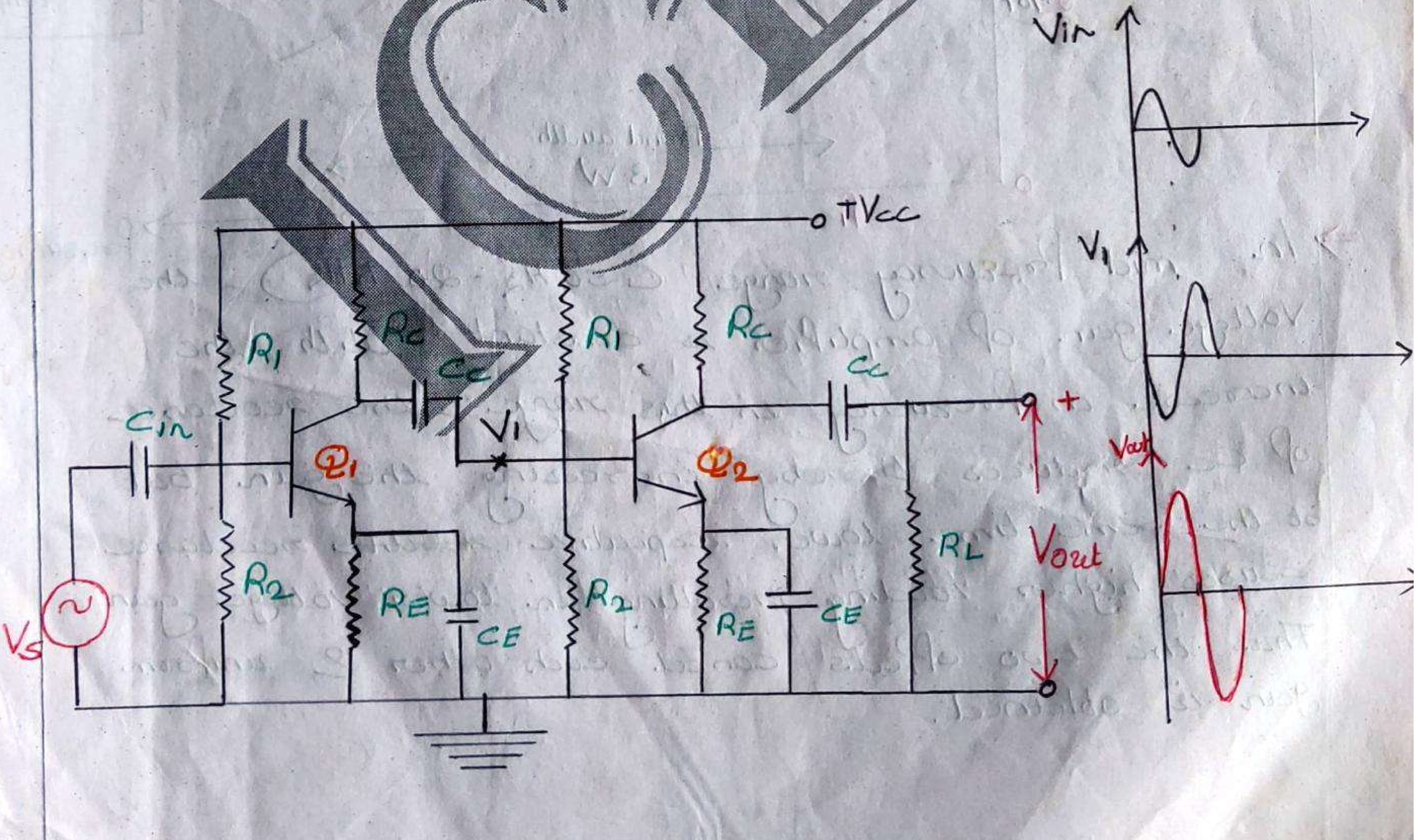
$$\therefore A_V = \frac{g_m (R_s \| R_L)}{1 + g_m (R_s \| R_L)}$$

Module: 3

R-C Coupled Amplifier

A two stage R-C coupled amplifier using N-P-N transistors in CE configuration is shown.

* 2 transistors are identical & use a common power supply V_{CC}.
* R_1, R_2 & R_E form biasing & stabilization.
* The signal developed across R_C of first stage is coupled to the base of second stage through C_C (coupling capacitor)
* C_E (emitter bypass capacitor) offers low reactance path.

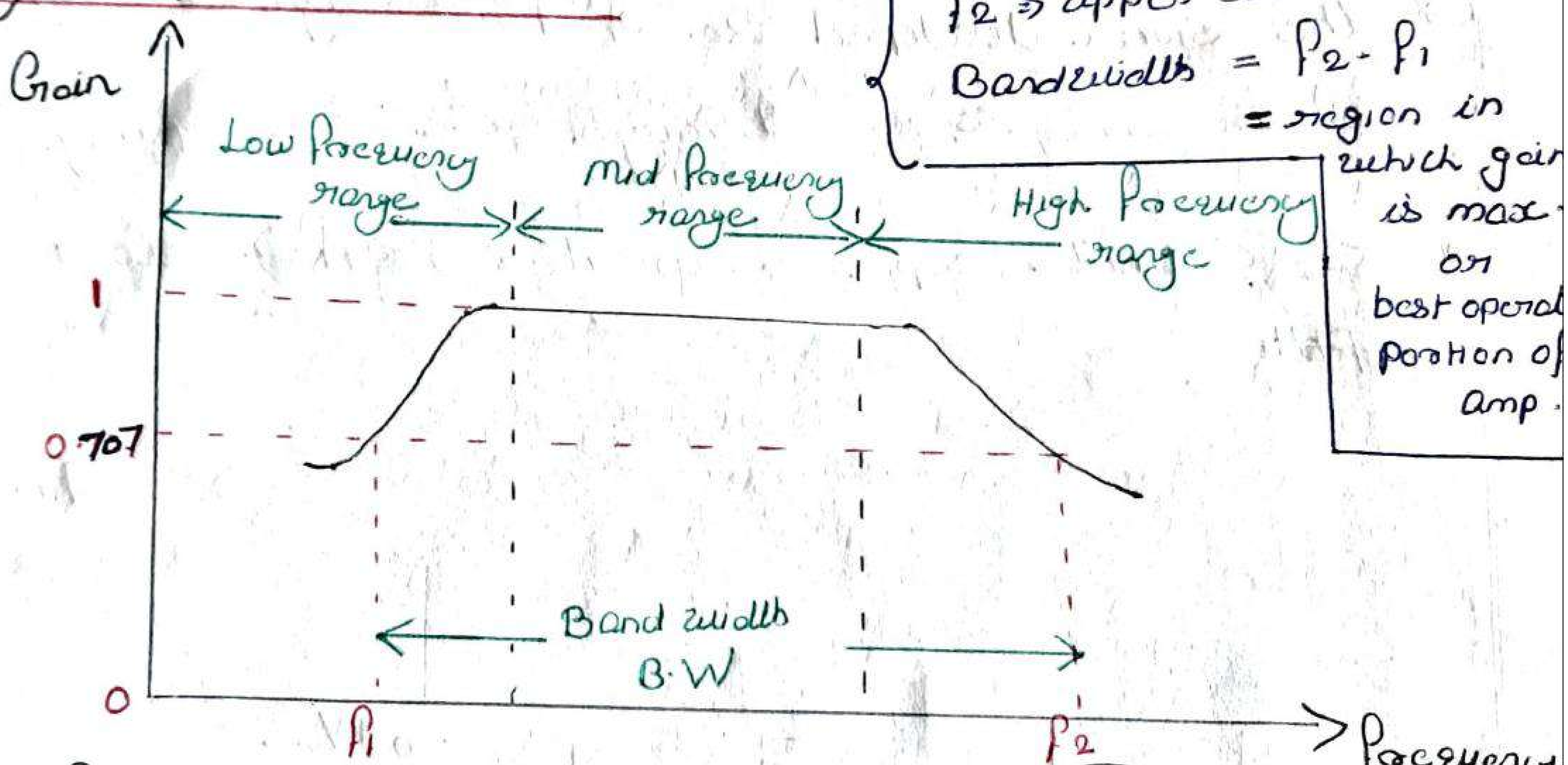


When ac signal is applied to the base first amplifier, it appears in the amplified form across collector load R_C. The amplified signal developed across R_C is transmitted to the base of next stage of amplifier through C_C. This is further amplified by next stage & so on. Thus the cascode stages amplify the signal & overall gain is increased. The phase of o/p is same as that of i/p.

important ... the ... are due ... junction

Frequency Response Curve

$f_1 \Rightarrow$ lower cut off freq
$f_2 \Rightarrow$ upper cut off freq
Bandwidth $= f_2 - f_1$
= region in which gain is max. or best operating portion of amp.



⇒ In mid frequency range (50 Hz - 20 KHz), the voltage gain of amplifier is constant. With the increase in frequency in this range, the reactance of C_C reduces thereby increasing the gain but at the same time lower capacitive ~~reactive~~ reactance causes higher loading resulting in lower voltage gain. Thus the two effects cancel each other & uniform gain is obtained.

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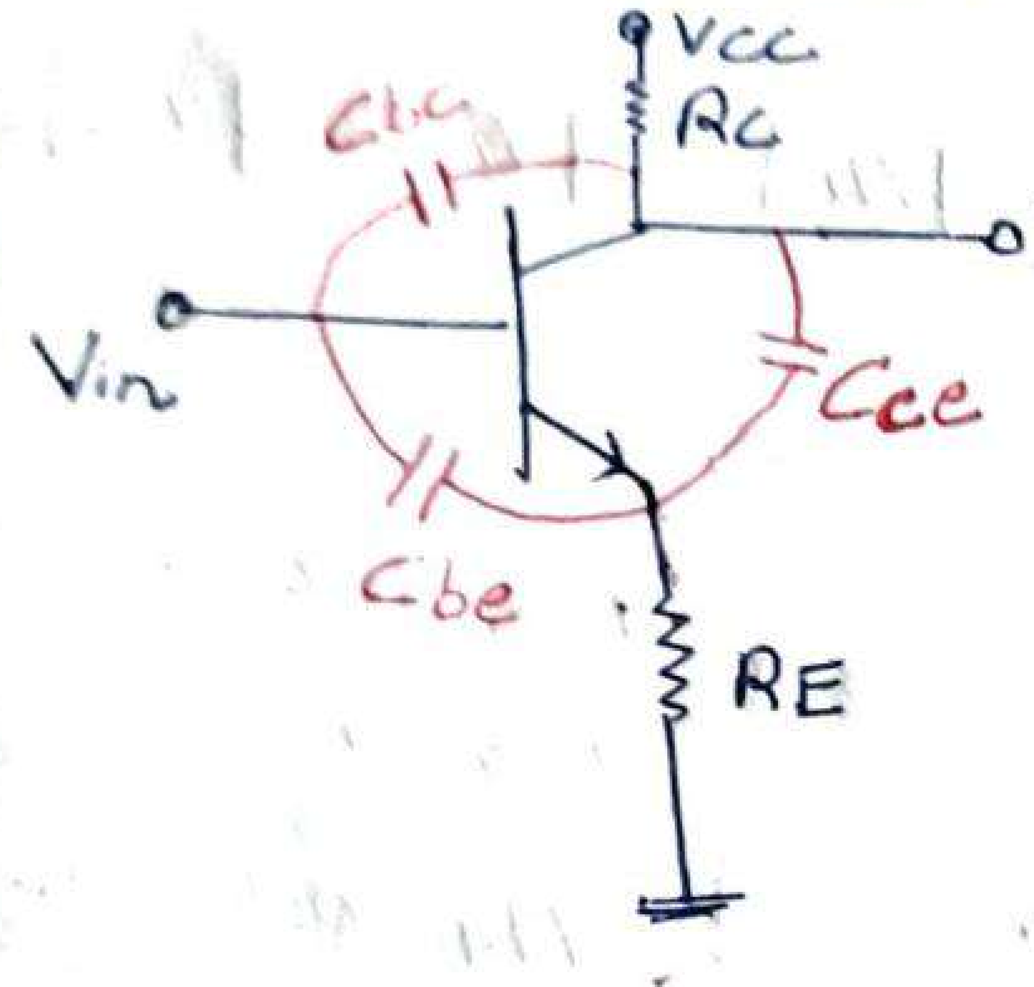
4)

The important factor that comes in high frequency is the interelectrode capacitances. These capacitances are due to formation of depletion layers at the junction. The interelectrode capacitance is shown,



At high frequency the reactance of Cbc, Cce & Cbe will be very low.

⇒ Reactance of $C_{bc} = 0$ (S.C)

o/p will be feedback to i/p (negative feedback) so gain is reduced. This effect is called Miller Effect

⇒ Reactance of $C_{be} = 0$ (S.C)

It offers a low impedance path to i/p signal & gain is reduced

⇒ Reactance of $C_{ce} = 0$ (S.C)

It cause shorting effect at o/p & gain reduces.

5)

Consider a 4 stage R.C coupled amplifier

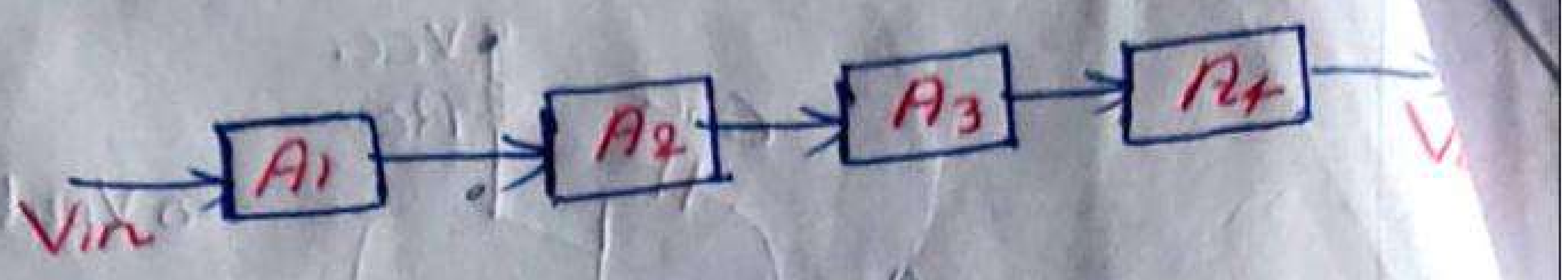
Let A_1 = gain of I^{st} stage

A_2 = " " II^{nd} "

A_3 = " " III^{rd} "

A_4 = " " IV^{th} "

A = Overall gain



At ideal condition

$$A = A_1 A_2 A_3 A_4$$

but Practically $A < A_1 A_2 A_3 A_4$

because of loading effect.

A_2 act as load of A_1

A_3 " " " " A_2

A_4 act as load of A_3

Advantages: Excellent freq. response

cheaper

compact

Disadvantages: Poor impedance matching

Application: It is widely used as voltage amplifier, because of poor impedance matching this type of coupling is not employed in final stages.

At low frequencies (below 50 Hz) higher capacitive reactance of C_C allows very small part of signal to pass from one stage to next & also because of higher reactance of C_E, the emitter resistor R_E is not effectively shunted. Thus voltage gain falls off at low frequencies

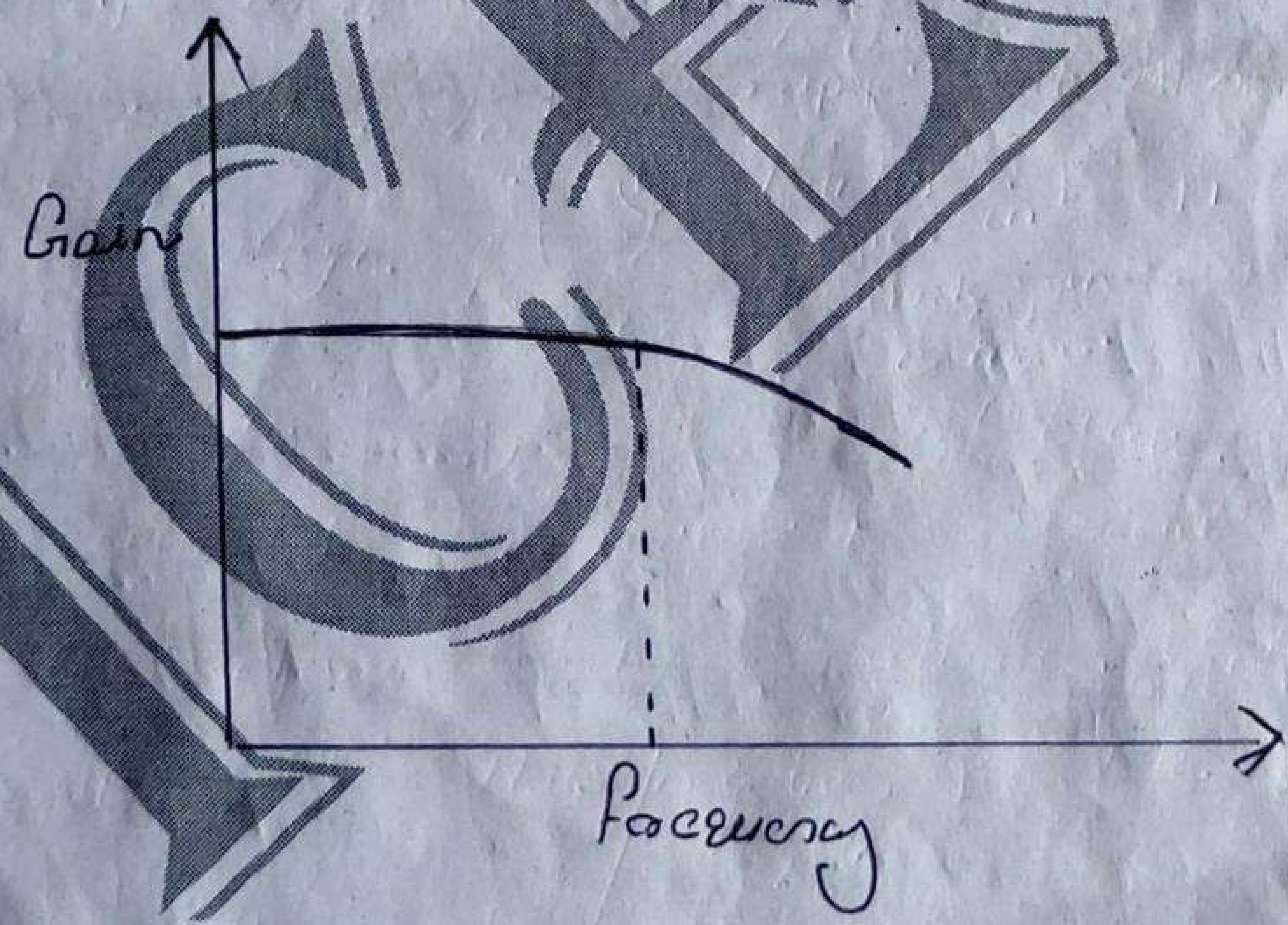
At high frequencies (exceeding 20 KHz), the gain of the amplifier decreases with the increase in frequency. Several factors are responsible for this reduction in gain. At high frequencies, the reactance of C_C becomes very small & C_C behaves as short-circuit. This increase the loading of next stage & reduces the voltage gain. At high frequencies, capacitive reactance of base emitter junction is low & so the base current is increased & current gain factor β is reduced. At high frequencies, the interelectrode capacitance C_{bc} connects the o/p ckt to i/p ckt. Thus negative f.b takes place & gain is reduced.

$$X_C = \frac{1}{2\pi f \cdot C}$$

eration : The weak signal is applied to the base of the transistor. Due to transistor action, an amplified output is obtained across the collector load R_{C1} of the first transistor. The amplified signal developed across R_{C1} is supplied to the base of next transistor. This is further amplified by next stage & so on.

Frequency Response.

It has no coupling & bypass capacitor to cause a drop at low frequency. The frequency response curve is flat upto upper cut-off frequency f_2. Above this gain decreases due to inter-electrode capacitance of device

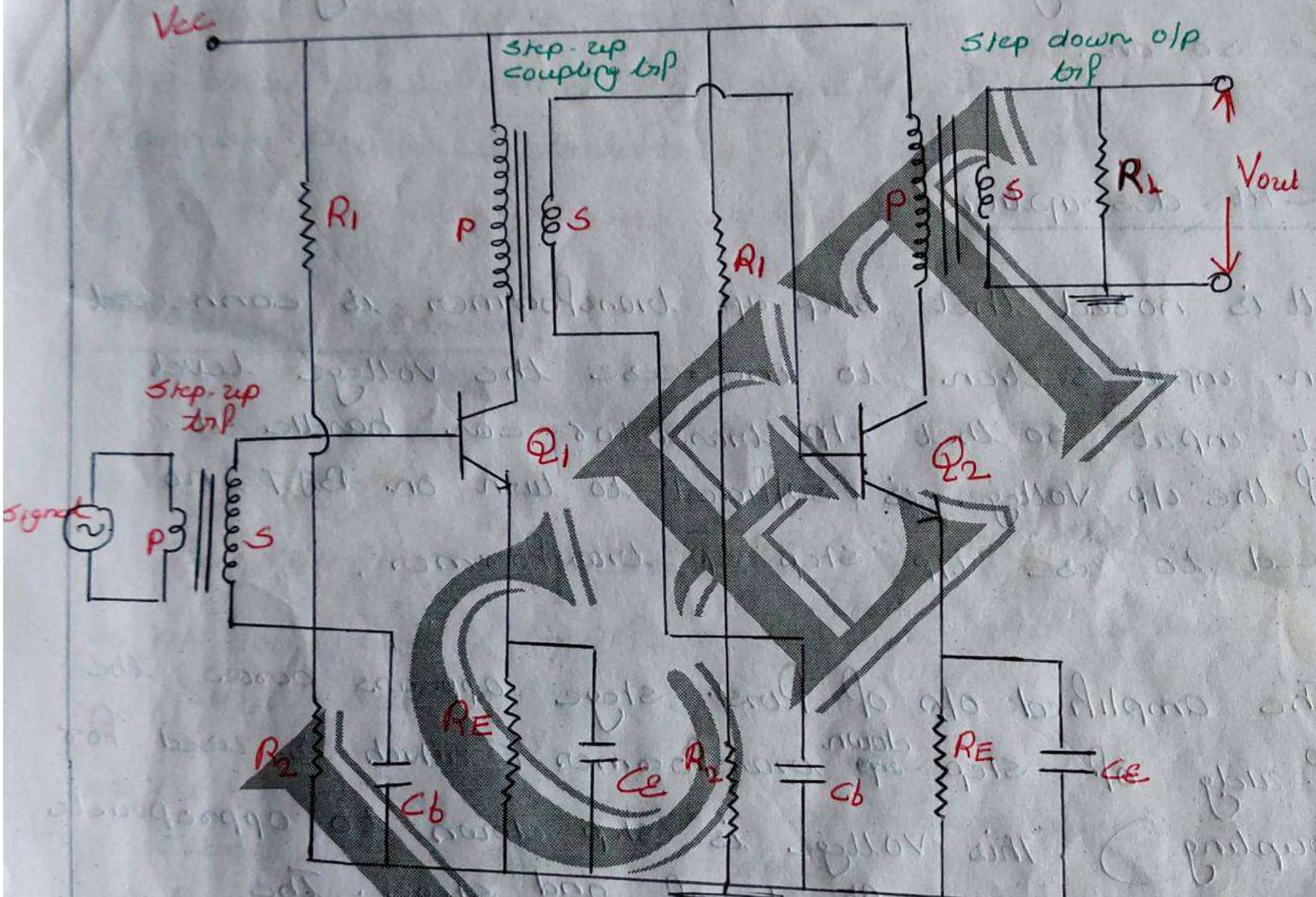


8)

Merits: Cheap,
can amplify very low frequency signal.

Demerits: can't amplify high frequency signal
It has poor temp. stability.

Transformer Coupled Transistor Amplifier



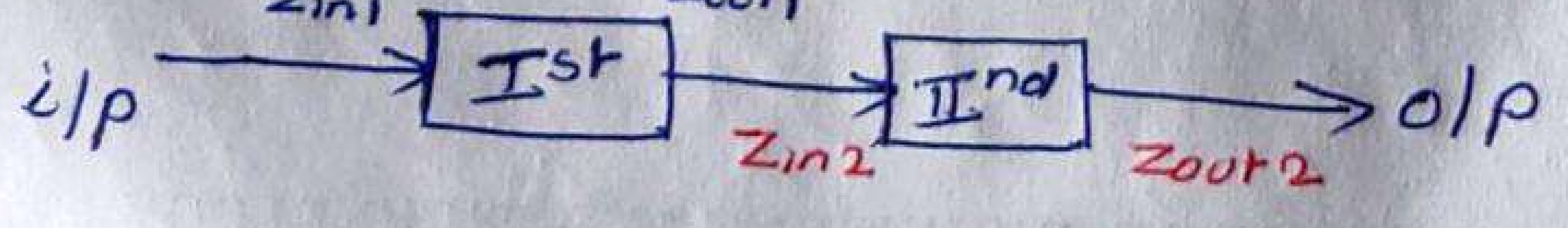
10)

operation : When the input ac signal is applied base of first transistor through step-up transform it gets amplified & appears across the primary coupling transformer. The voltage developed across the primary is transferred to the i/p of next stage. The second stage further amplifies in an exactly similar way & so on.

<u>Ckt description</u>

⇒ It is noted that step-up transformer is connected in input section, to increase the voltage level at input, so that i/p transistor can handle it. If the i/p voltage is sufficient to turn on BJT, no need to use i/p step up transformer.

⇒ The amplified o/p of first stage appears across the 1° wdg of step-~~up~~ down transformer (which is used for coupling). This voltage is step-down to appropriate voltage & is given as i/p of 2nd stage. The step down transformers are used for coupling because
1) To adjust or reduce the o/p of I^{st} stage to a proper value so that next stage can be easily handled
2) For impedance matching.



Impedance matching means, when we cascade different stages the o/p imp. of a stage should match with i/p imp of next stage.
We can achieve this impedance matching by step-down transformers by adjusting its turn's ratio.
Maximum power is transfered if $Z_{out_1} = Z_{in_2}$
{Maximum power transfer theorem}

Frequency Response.

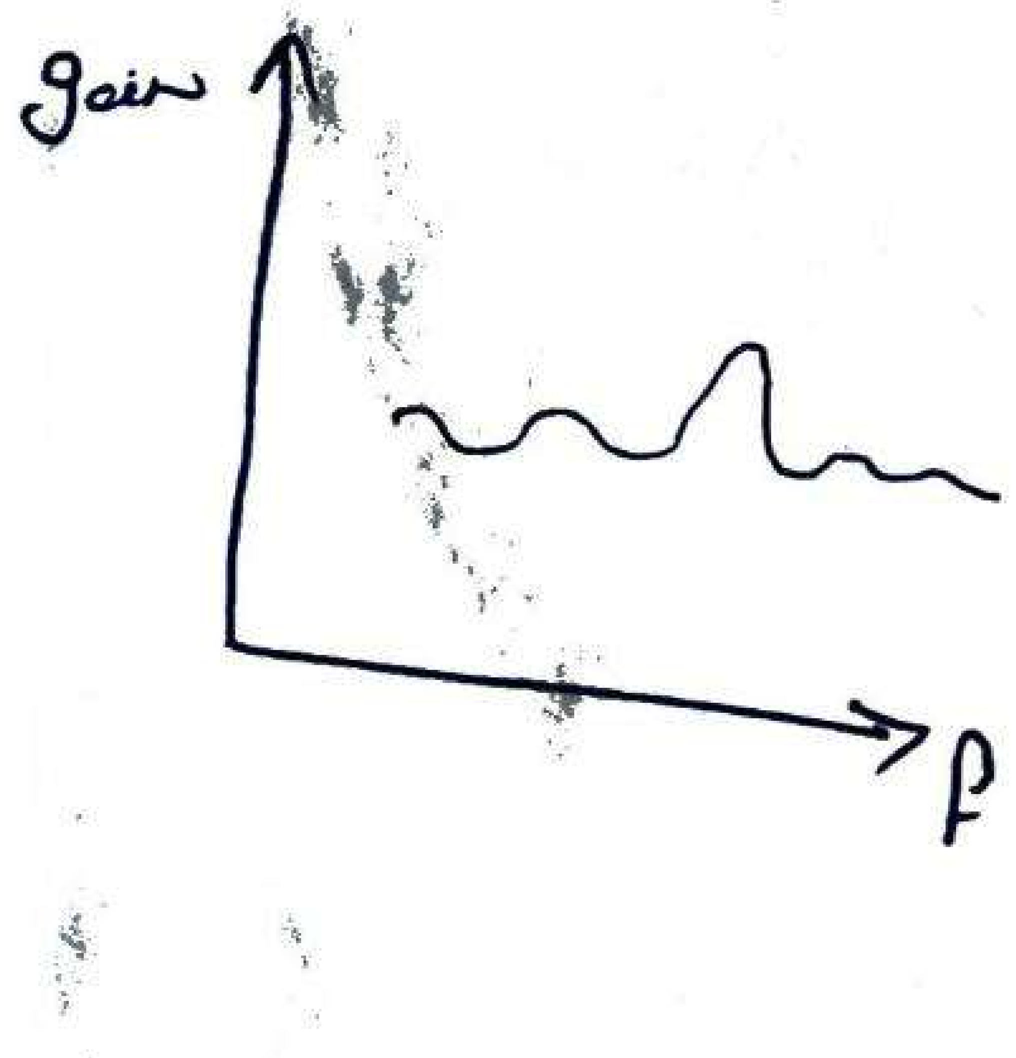
The frequency response of trf-coupled amplifier is very poor.

The o/p Voltage $= I_C \times X_L$

⇒ At low freq, $X_L = 2\pi f L$ = low, so o/p is low & gain is reduced.

⇒ At high freq, the winding inter capacitance's effect came, & so gain is reduced.

But at resonance condition the gain will be maximum



Advantages: 1) low dc resistance at collector
2) best impedance matching.
3) coupling is effective

Disadvantages: 1) Poor frequency response.
2) Bulky & costly.

Applications: It is not used for amplifying low freq. signal. It is used for radio frequency (20 kHz <) amplification.

Power Amplifier Stages

Power amplifier is meant to amplify a weak signal until sufficient power is available to operate an output device such as a loudspeaker, a solenoid or a relay. Power amplifier, to provide the desired power amplification, has generally 3 stages

1. Voltage Amplification stage

⇒ For raising the level of weak i/p signal, it is amplified in two or more stages, R-C coupling is usually employed.

2) Driver stage

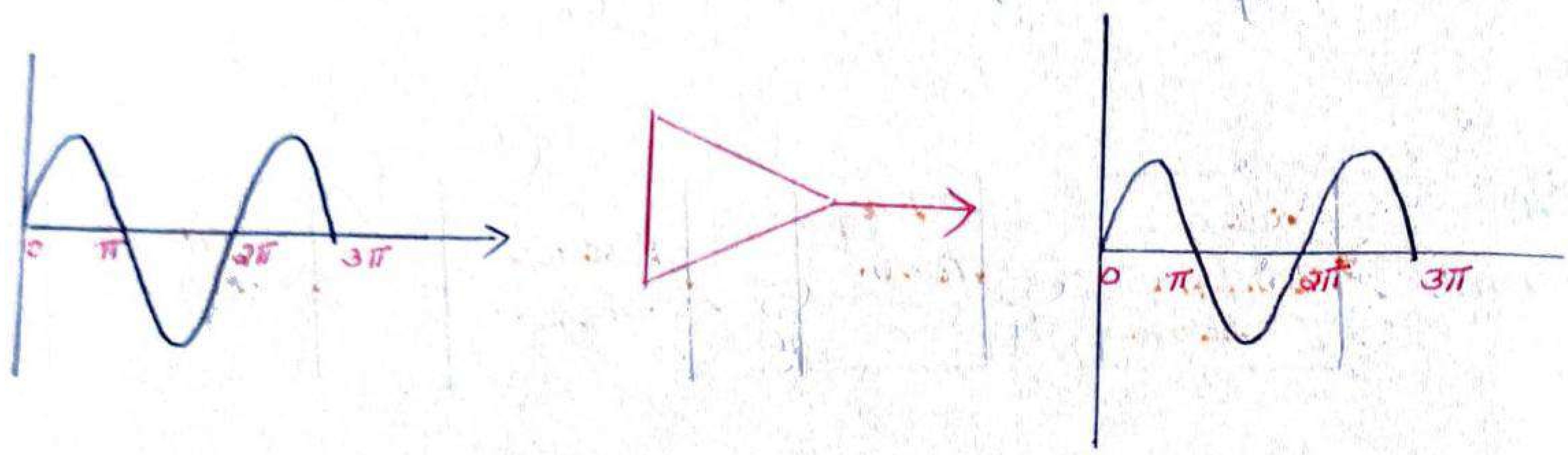
⇒ The stage that precedes the o/p stage is called the driver stage. The driver stage renders power amplification.

3) Output stage

⇒ The o/p stage essentially consists of a power amplifier & is meant for transferring maximum power to o/p device.

Class A power amplifier

A class A power amplifier is defined as a pow
amplifier in which o/p current flows for the full-cyc
(360°) of the i/p signal. In other words, the
transistor remains forward biased throughout the
i/p cycle.



⇒ o/p current flows for entire 360° of i/p cycle

⇒ transistor remains forward biased through out i/p cycle

⇒ The Q-pt is located at middle of load line

⇒ o/p contains less distortion.

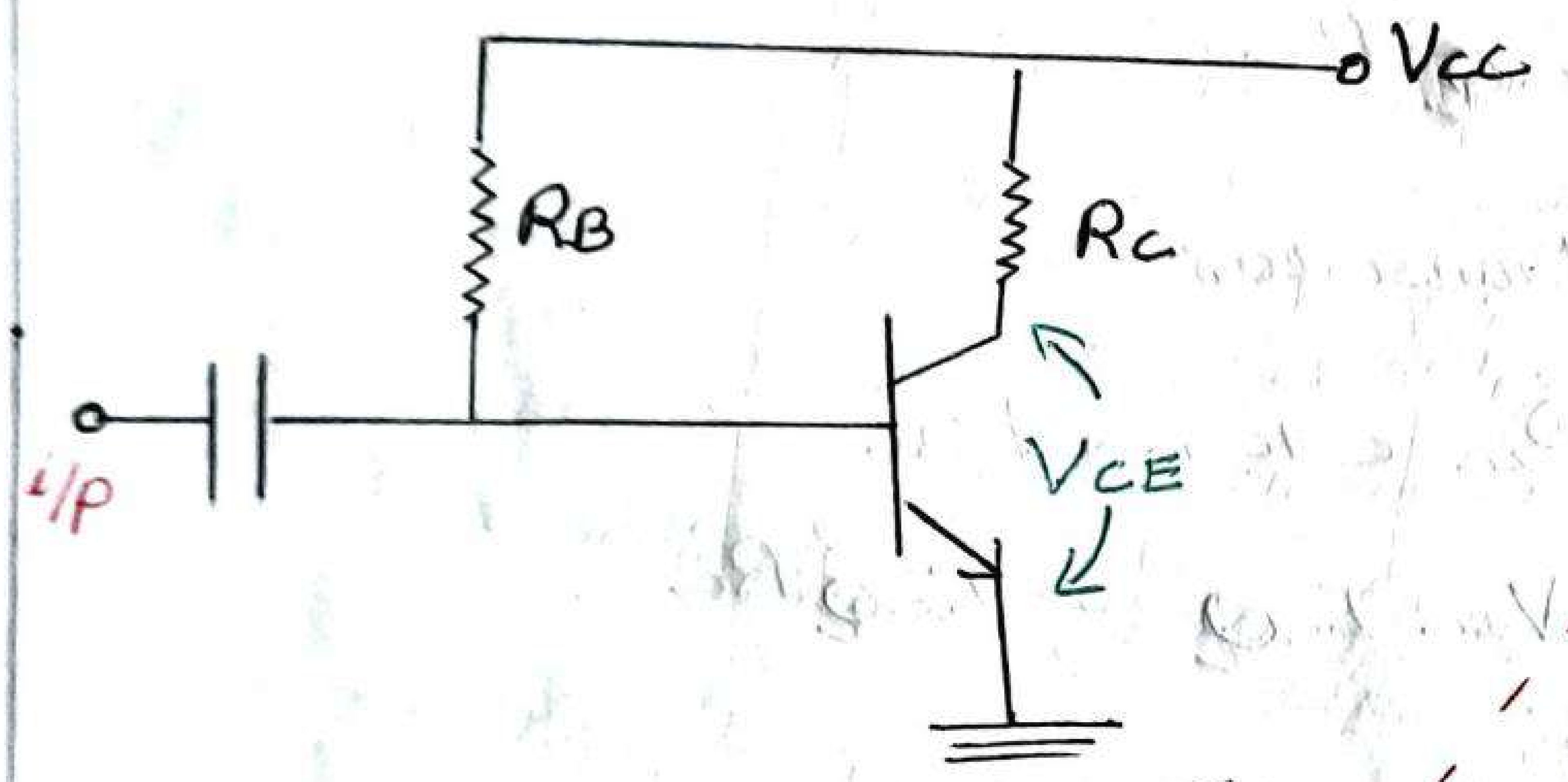
Two types of class A power amplifier.

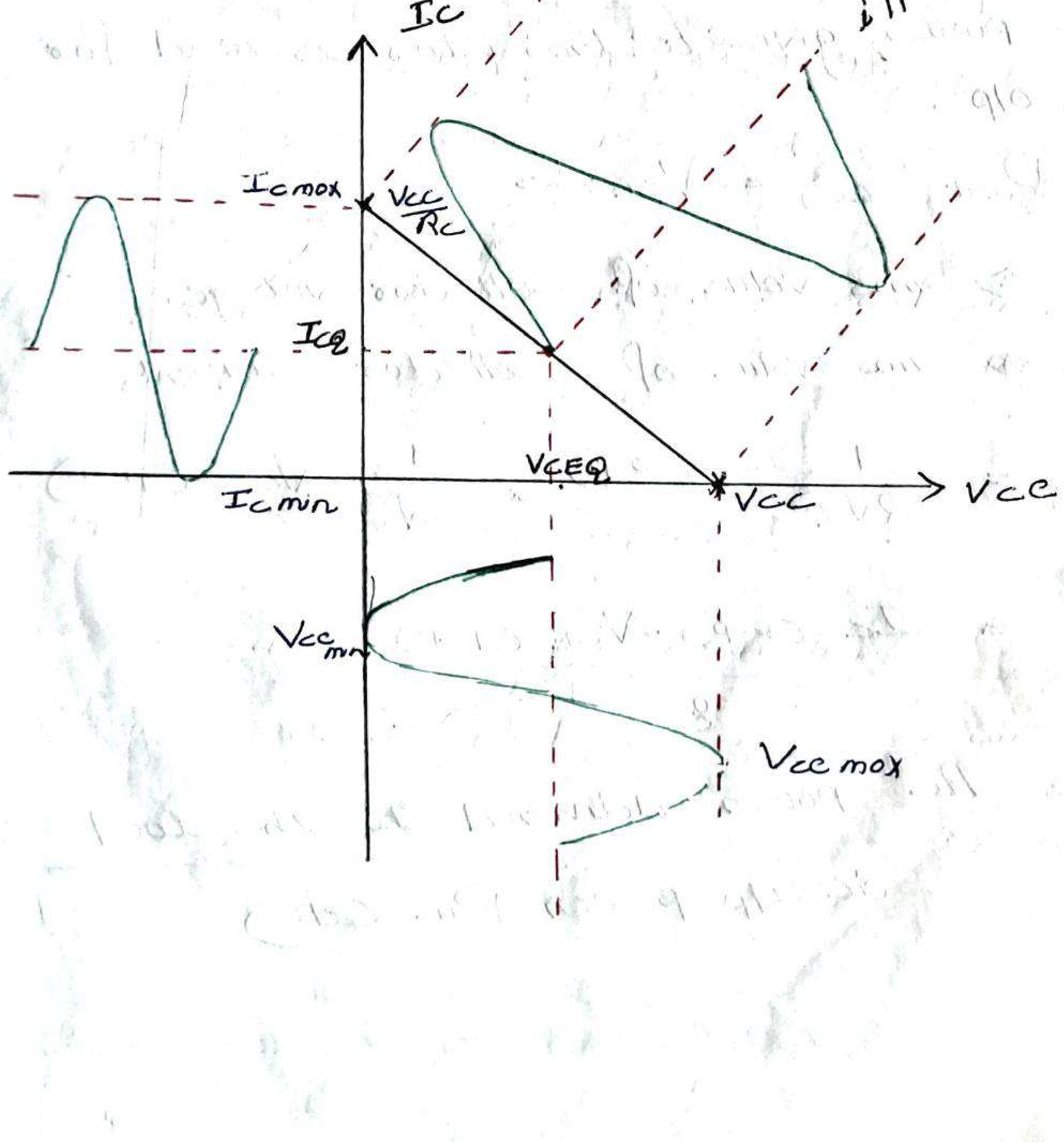
1) Series fed class A power amplifier

2) Transformer coupled class A power amplifier

Series fed class A power amplifier

The load resistance R_c is connected in series with the transistor o/p. The i/p signal used is in the range of volts & the transistor used is power transistors.





input power from the supply.

$$P_{in}(dc) = V_{cc} \cdot I_{cQ}.$$

this power is used in the following components

1) Power dissipated across collector

$$P_{RC} = I_{cQ}^2 R_C$$

2) Power to transistor

$$P_{tr} = P_{in}(dc) - P_{RC}$$
$$= V_{cc} I_{cQ} - I_{cQ}^2 R_C$$

The power given to transistor is used for developing the o/p.

$$P_{out}(ac) = V_{CE} \cdot I_C$$

$V_{CE} \Rightarrow$ rms value of collector voltage

$I_C \Rightarrow$ rms value of collector current

$$= \frac{1}{2\sqrt{2}} I_C(P\text{-}P) \times \frac{1}{2\sqrt{2}} V_{CE}(P\text{-}P)$$

$$= \frac{I_C(P\text{-}P) \cdot V_{CE}(P\text{-}P)}{8}$$

$$\eta = \frac{\text{AC power delivered to the load}}{\text{dc i/p power } P_{in}(dc)}$$

CP-P) CE CP AC

$I_C(P\text{-}P) = \frac{V_{cc}}{R_c}$

$V_{CE}(P\text{-}P) = V_{cc}$

$P_{ac}\ o/p = \frac{\frac{V_{cc}}{R_c} \cdot V_{cc}}{8} = \frac{V_{cc}^2}{8R_c}$

$\eta = \frac{V_{cc}^2/8R_c}{V_{cc}^2/2R_c} = 2/8 = 0.25$ or $\underline{\underline{25\%}}$

Collector efficiency $\eta = \frac{P_{out}(ac)}{P_{tr}(dc)}$

$P_{tr}(dc) = V_{cc}I_{cQ} - I_{cQ}^2 R_c$

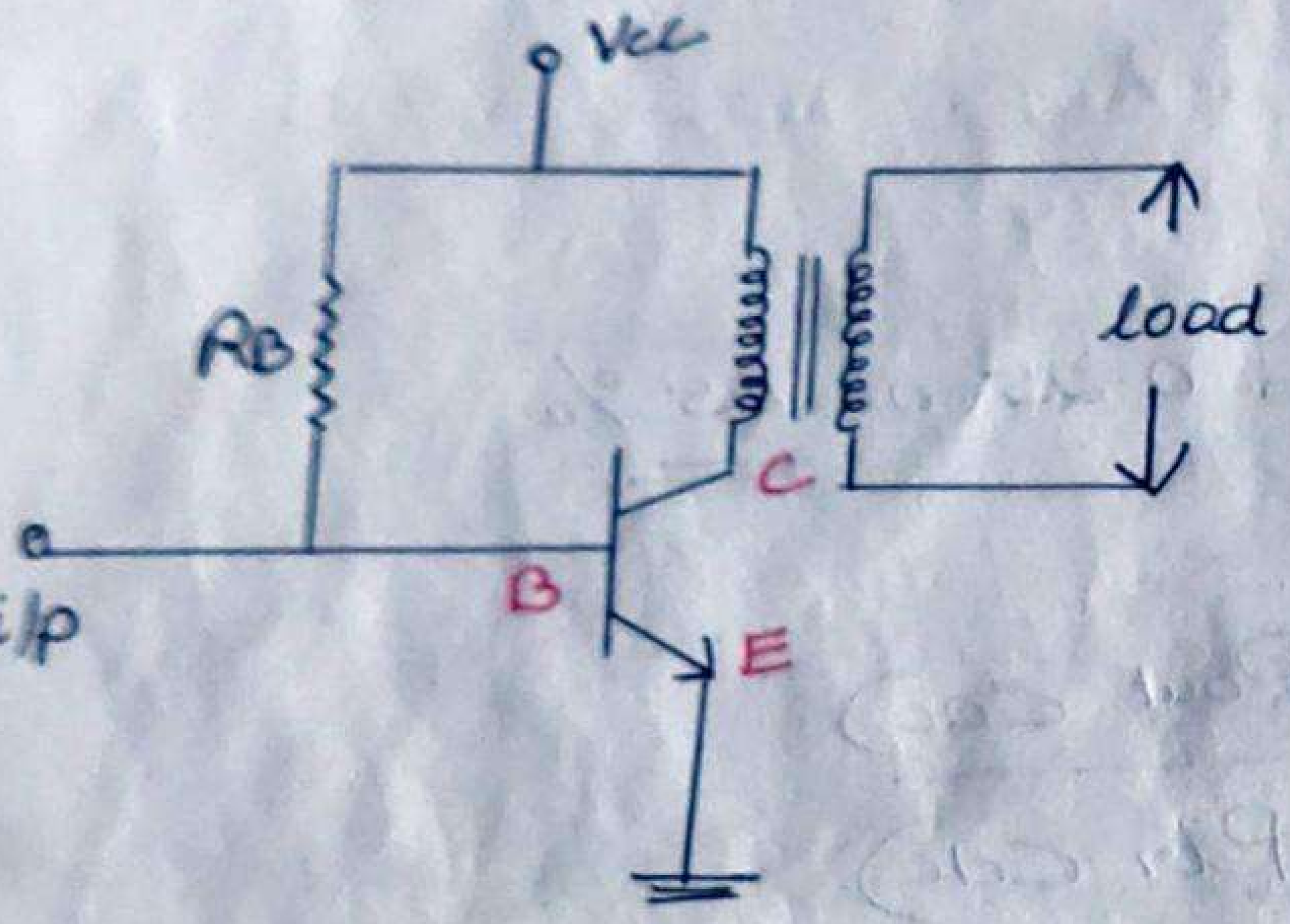
$= V_{cc} \cdot \frac{V_{cc}}{2R_c} - \frac{V_{cc}^2}{4R_c^2} R_c$

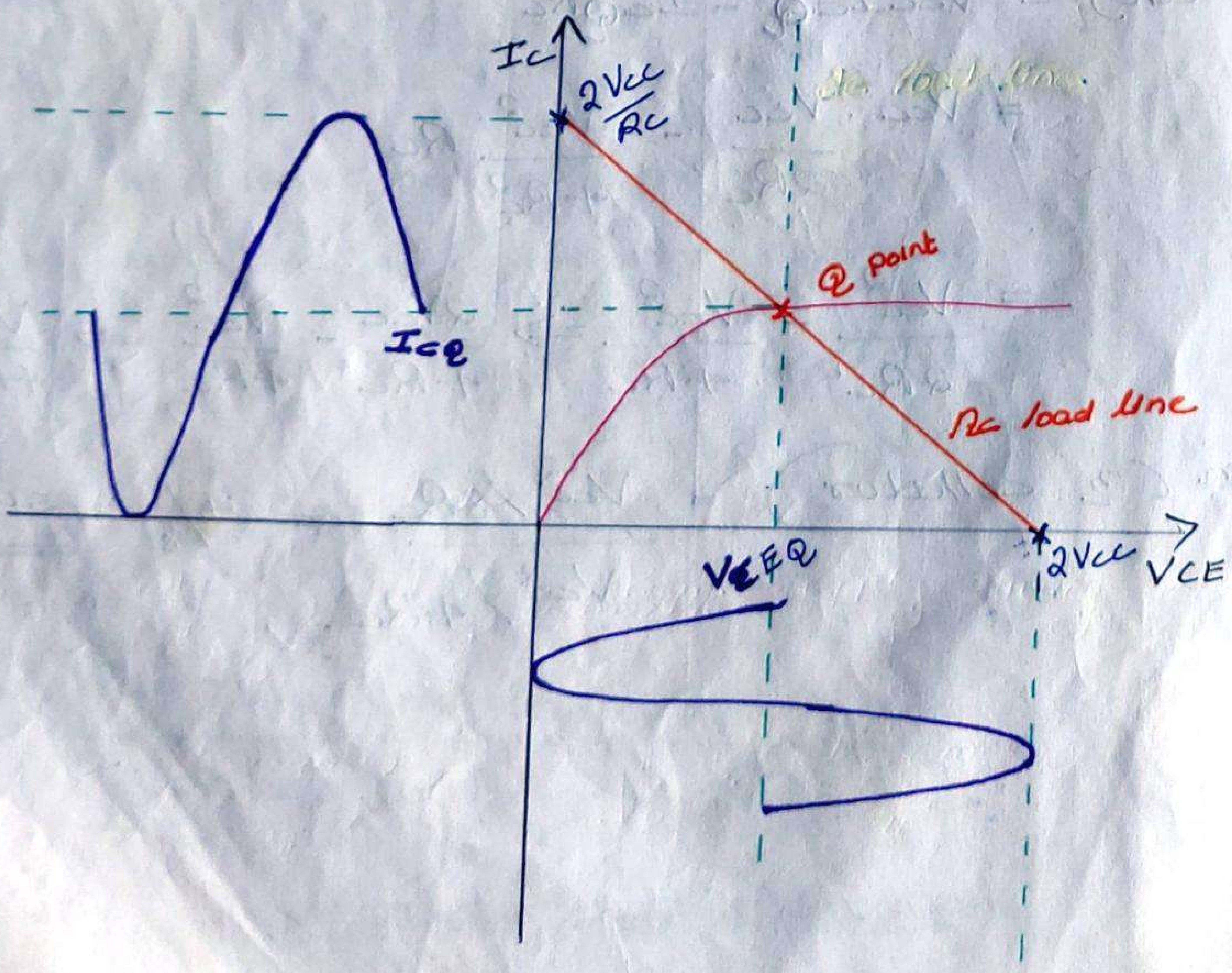
$= \frac{V_{cc}^2}{2R_c} - \frac{V_{cc}^2}{4R_c} \Rightarrow \frac{2V_{cc}^2}{4R_c} - \frac{V_{cc}^2}{4R_c} \Rightarrow \frac{V_{cc}^2}{4R_c}$

then $(\eta\ \text{collector}) = \frac{V_{cc}^2/8R_c}{V_{cc}^2/4R_c} = 4/8 = \underline{\underline{50\%}}$

2) Transformer Coupled Class A power Amplifier

In series fed class A power amp, the collector resistor causes large wastage of power. In order to avoid this wastage of power we are using the transformer coupled power amplifier.





The dc winding resistance determines the DC load line, this is quite small. DC load line is a straight line rising from V_{cc}.

I_c changes from 0 to $2I_{CQ}$

V_{CE} changes from 0 to $2V_{cc}$.

In ideal transformer, there is no voltage drop in primary so

$$V_{cc} = V_{CEQ}.$$

So $P_{tr} = P_{in}(dc) = V_{cc} \cdot I_{CQ}$

Overall Efficiency = Collector efficiency

$$\frac{P_{out}(ac)}{P_{tr}} = \frac{P_{out}(ac)}{V_{cc} \cdot I_{CQ}}$$

$$P_{out}(ac) = V^{CE}_{rms} \cdot I^{C}_{rms}$$

$$= \frac{1}{2\sqrt{2}}\left[V_{ce(max)} - V_{ce(min)}\right] \times \frac{1}{2\sqrt{2}}\left[I_{C(max)} - I_{C(min)}\right]$$

$$= \frac{1}{2\sqrt{2}}\left[2V_{cc} - 0\right] \times \frac{1}{2\sqrt{2}}\, 2I_{CQ}$$

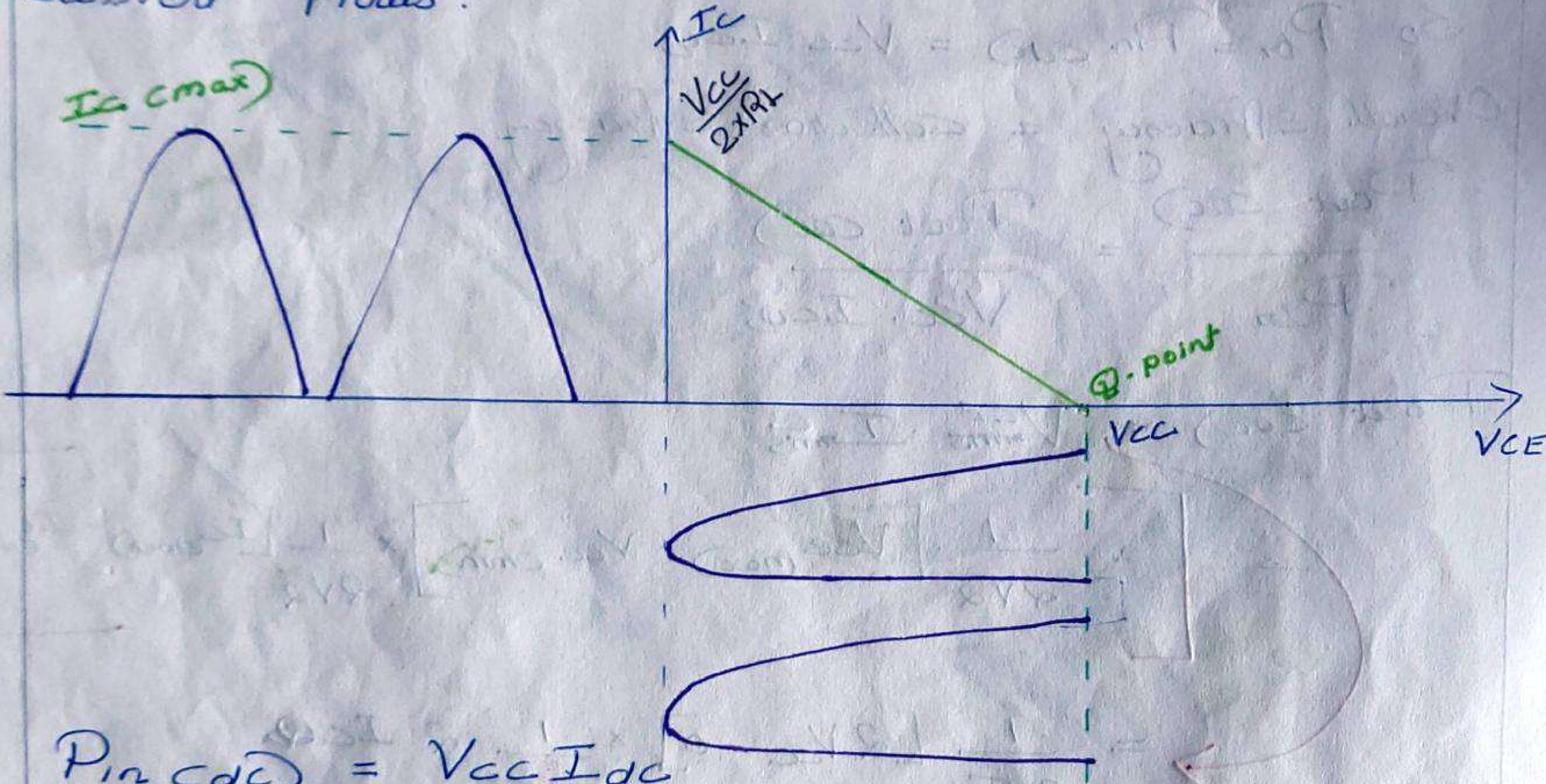
$$= \frac{V_{cc}}{\sqrt{2}} \times \frac{I_{CQ}}{\sqrt{2}} = \frac{V_{cc}\, I_{CQ}}{2}$$

$$\eta = \frac{P_{out}(ac)}{P_{in}(dc)} = \frac{V_{cc}\, I_{CQ}/2}{V_{cc} \times I_{CQ}} = 50\%$$

Class B power Amplifier

The transistor is so biased that the zero signal collector current is zero. The Q-pt is set at the cut off region. It remains forward biased for only one half cycle of the i/p signal. It's conduction angle is 180°.

During the half cycle of i/p signal, the ckt is forward biased & the collector current flows. On the otherhand during -ve half cycle of i/p ac signal, the ckt is reverse biased & no current flows.



$P_{in}(dc) = V_{CC} I_{dc}$

$I_{dc} \Rightarrow$ avg current taken from supply during ON condition

$$I_{dc} = \frac{1}{2\pi}\int_0^{\pi} I_{c(max)} \sin\theta \, d\theta$$

$$= \frac{I_{c(max)}}{2\pi}\Big[-\cos\theta\Big]_0^{\pi} = \frac{I_{c(max)}}{\pi}$$

$$P_{in}(dc) = \frac{V_{cc} I_c(max)}{\pi}$$

$$P_{out}(ac) = \frac{1}{2}(V_{rms} \times I_{rms})$$

o/p flows only one half cycle

$$V_{rms} = \frac{V_m}{\sqrt{2}} \; ; \; I_{rms} = \frac{I_c(max)}{\sqrt{2}}$$

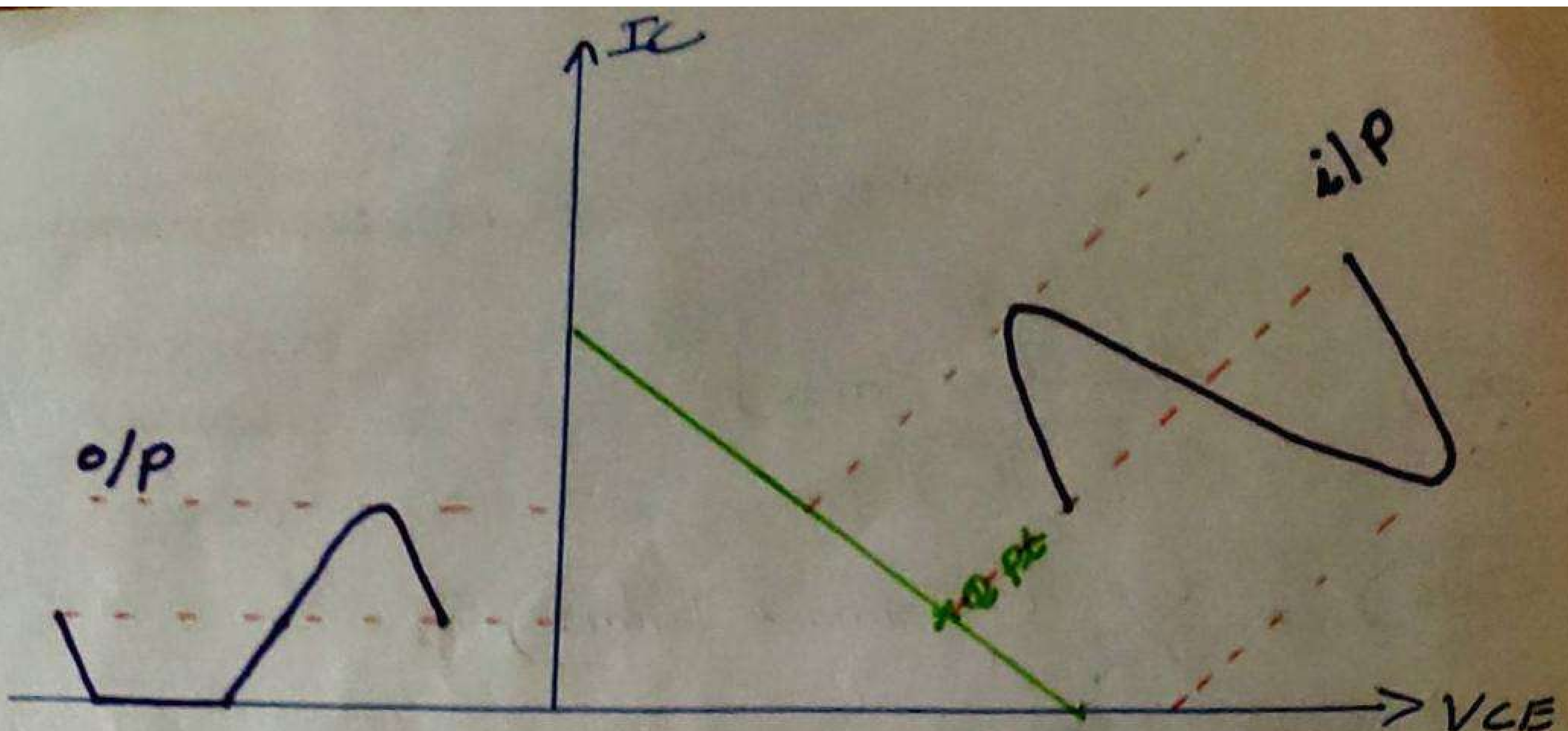
$$P_{out}(ac) = \frac{1}{2}\left[\frac{V_{cc}}{\sqrt{2}} \cdot \frac{I_c(max)}{\sqrt{2}}\right] = \frac{V_{cc} \cdot I_c(max)}{4}$$

$$\eta = \frac{P_{out}(ac)}{P_{in}(dc)} = \frac{V_{cc} \cdot \frac{I_c(max)}{4}}{V_{cc} \cdot \frac{I_c(max)}{\pi}} = \pi/4 = \underline{\underline{78.5\%}}$$

Class AB power amplifier

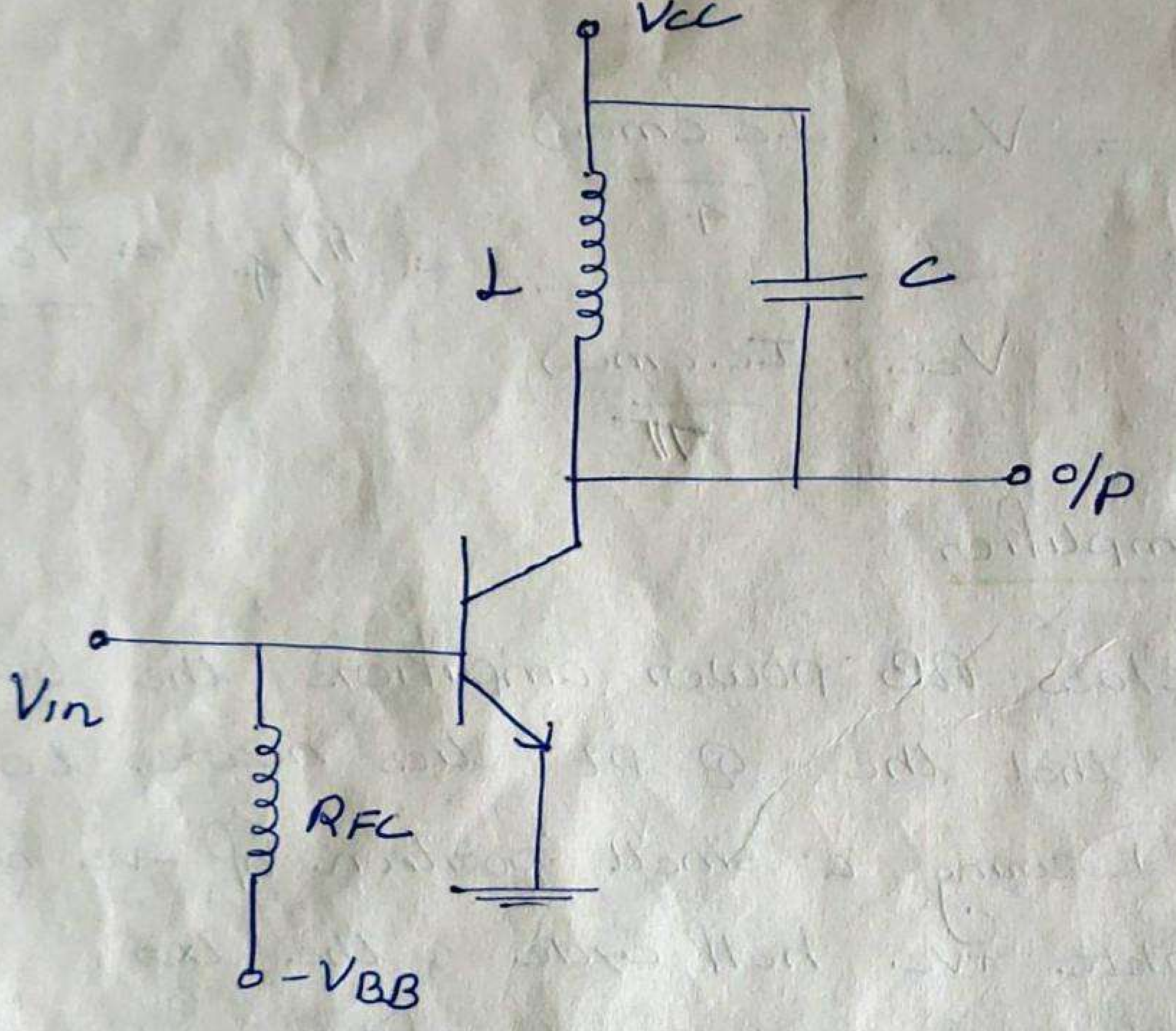
In class AB power amplifiers the biasing ckt is so adjusted that the Q-pt lies nearer to cut-off region. During a small portion of -ve half cycle & for complete +ve half cycle, the txr remains forward biased & the o/p flows.

During a small portion of -ve half cycle the txr is reverse biased & no current ~~current~~ flows through ckt.



Class C power amplifier

It is biased to operate for less than 180° of i/p signal



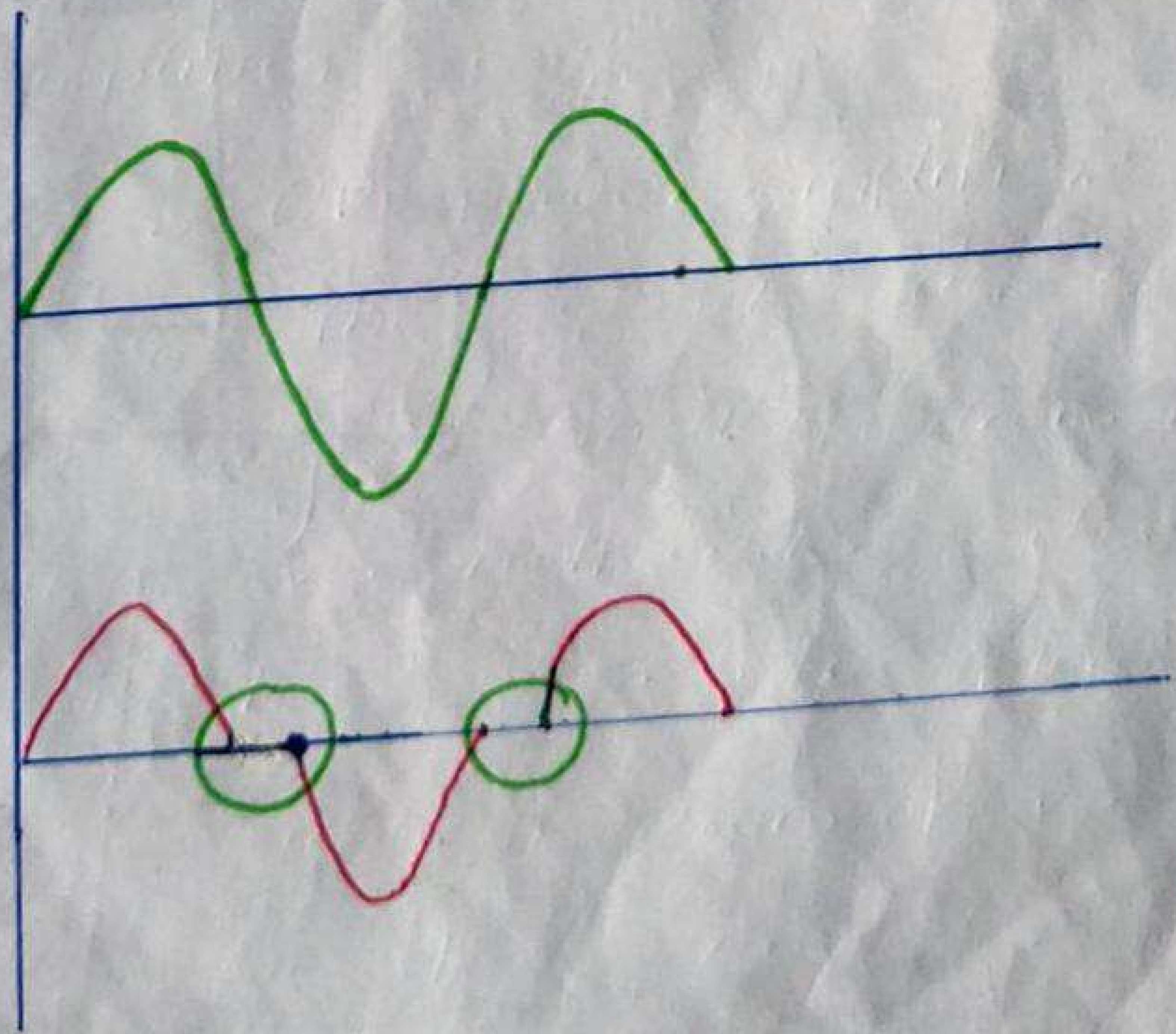
i/p

Harmonic Distortion

It is due to the non linearity of txr. It increases as we go from class A to class C.
Either non linear distortion is present, the o/p waveform contains components of frequencies which are harmonics of i/p signal frequency.

Cross Over distortion

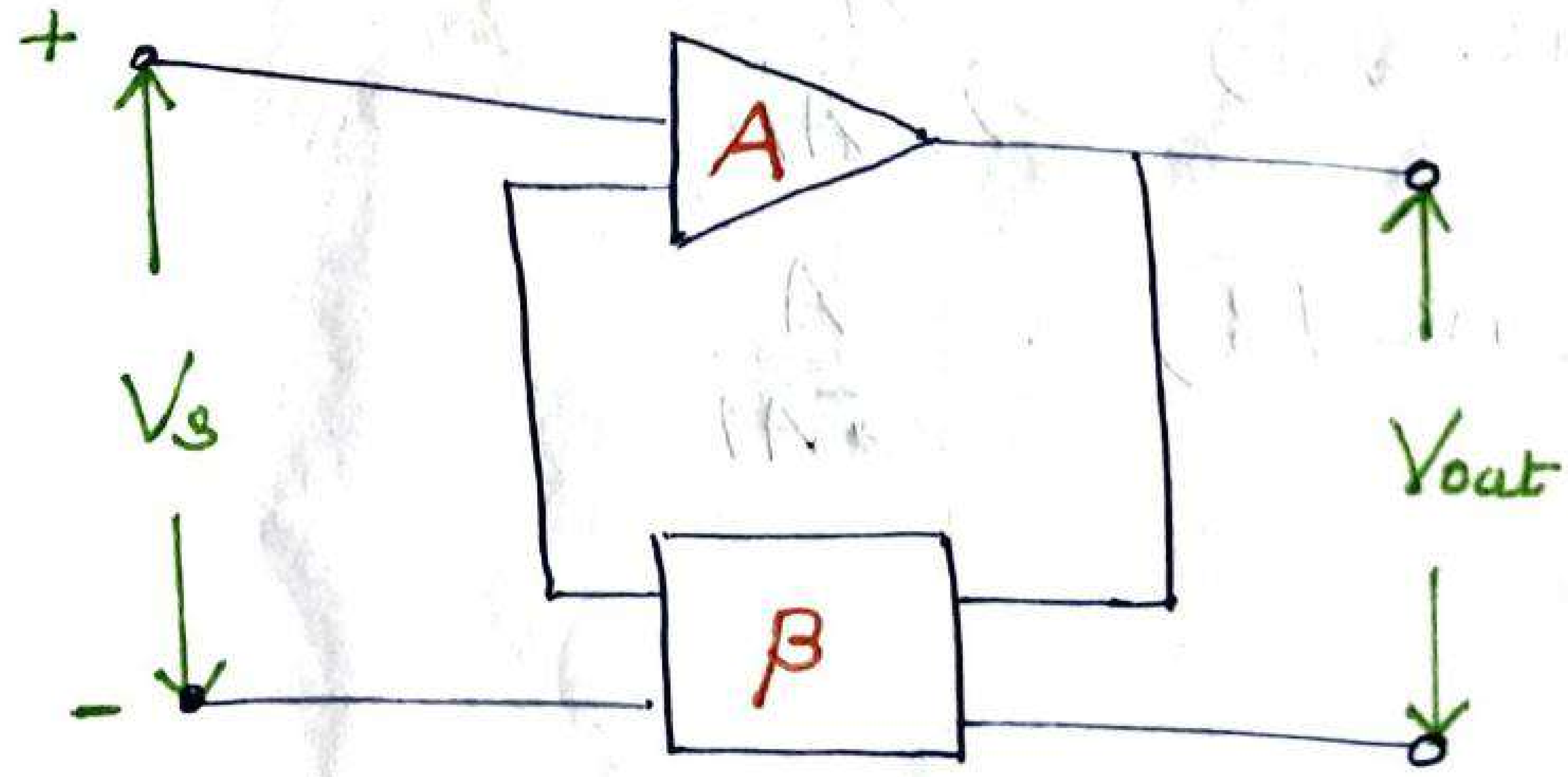
In silicon txr, at least 0.6V is required for conduction. In push pull amplifiers, the forward bias is produced by the i/p & both of the txr will be in off condition, when the i/p is less than ±0.5V. This introduces the crossover distortion in the o/p.



Feed Back Amplifiers

The voltage gain, i/p impedance, o/p impedance, B.W etc are some of the important characteristic of an amplifier. These parameters can be controlled by using the f.b technique

Process of combining a fraction of o/p back to the i/p is called the feedback; when the f.b voltage is applied in phase with the i/p signal, it is called positive or regenerative f.b. When the fb signal is applied in phase opposite to the i/p signal is called negative or degenerative f.b.



$A \Rightarrow$ gain of open loop a

$\beta \Rightarrow$ feedback ratio

$V_f \Rightarrow$ feedback voltage

$V_s \Rightarrow$ i/p signal

$A\beta \Rightarrow$ feedback factor

For positive f.b ; $V_{in} = V_s + V_f$

negative f.b ; $V_{in} = V_s - V_f$

Gain of openloop amplifier $A = \dfrac{V_{out}}{V_{in}}$

the f.b factor $\beta = \dfrac{V_f}{V_{out}}$

then $V_f = \beta V_{out}$

for negative feedback, $V_{in} = V_s - V_f$

$$V_{in} = V_s - \beta V_{out}$$

then $V_{out} = A V_{in}$

$$= A\left[V_s - \beta V_{out}\right]$$

$$V_{out} = A V_s - A\beta V_{out}$$

$$V_{out}\left[1 + A\beta\right] = A V_s$$

then the overall voltage gain $= \dfrac{V_{out}}{V_s}$

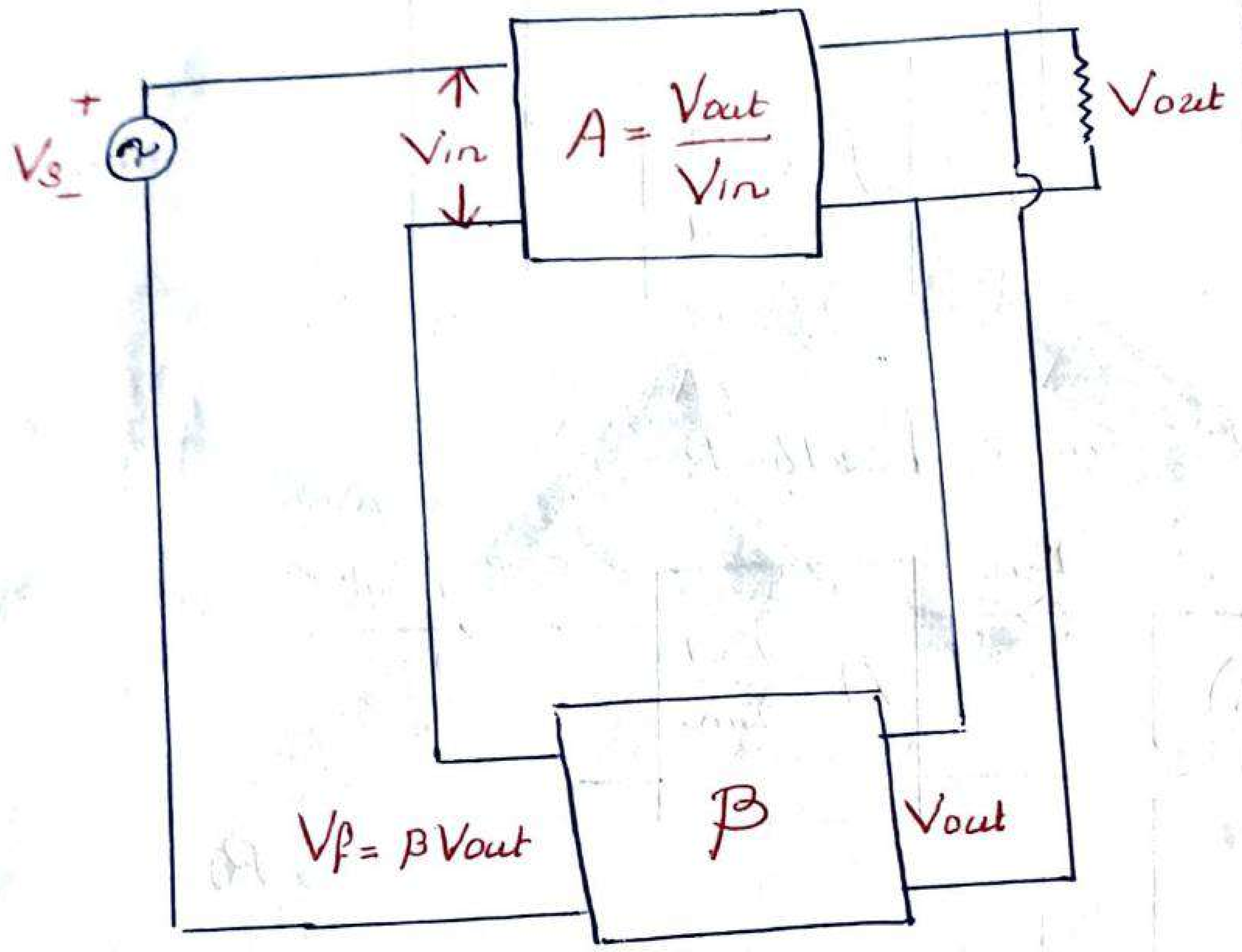
From the above equation $\dfrac{V_{out}}{V_s} = \dfrac{A}{1 + A\beta}$

Overall Voltage gain (-ve f.b) $= \dfrac{A}{1 + A\beta}$

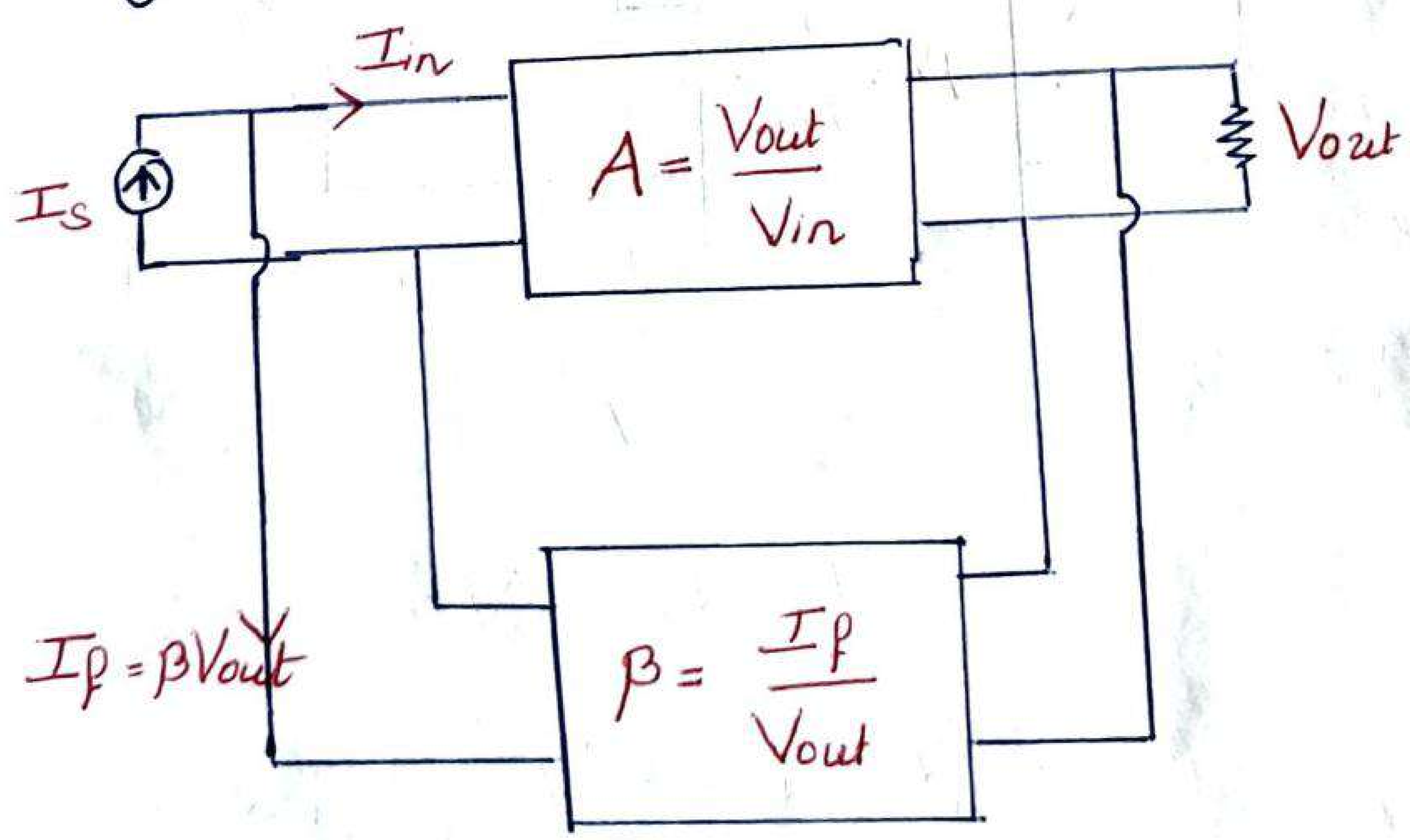
Overall Voltage gain (+ve f.b) $= \dfrac{A}{1 - A\beta}$

Types of feedback connection

a) Voltage series feedback



b) Voltage shunt feed back.



Advantages Of Negative Feedback

There are numerous advantages of negative feedback.

1) Gain stability

If we are using negative f.b, the gain of amplifier is

$$A_f = \frac{A}{1+A\beta}$$

if $A\beta \gg 1$; $A_f = 1/\beta$

The overall gain of amplifier is independent of the internal gain & depends only on β.
β is turn depends on the passive elements such as resistors.

2) Reduced Noise

The noise voltage in the amplifier is reduced by the factor $(1+A\beta)$ when the negative f.b is used

3) Increased B.W

The gain - B.W Product is const.

$A \times B.W$ = Constant.

if the -ve fb is used, the gain is reduced so B.W is improved.

4) Increases the i/p impedance

The i/p imp. of amplifier is increased by $(1+A\beta)$

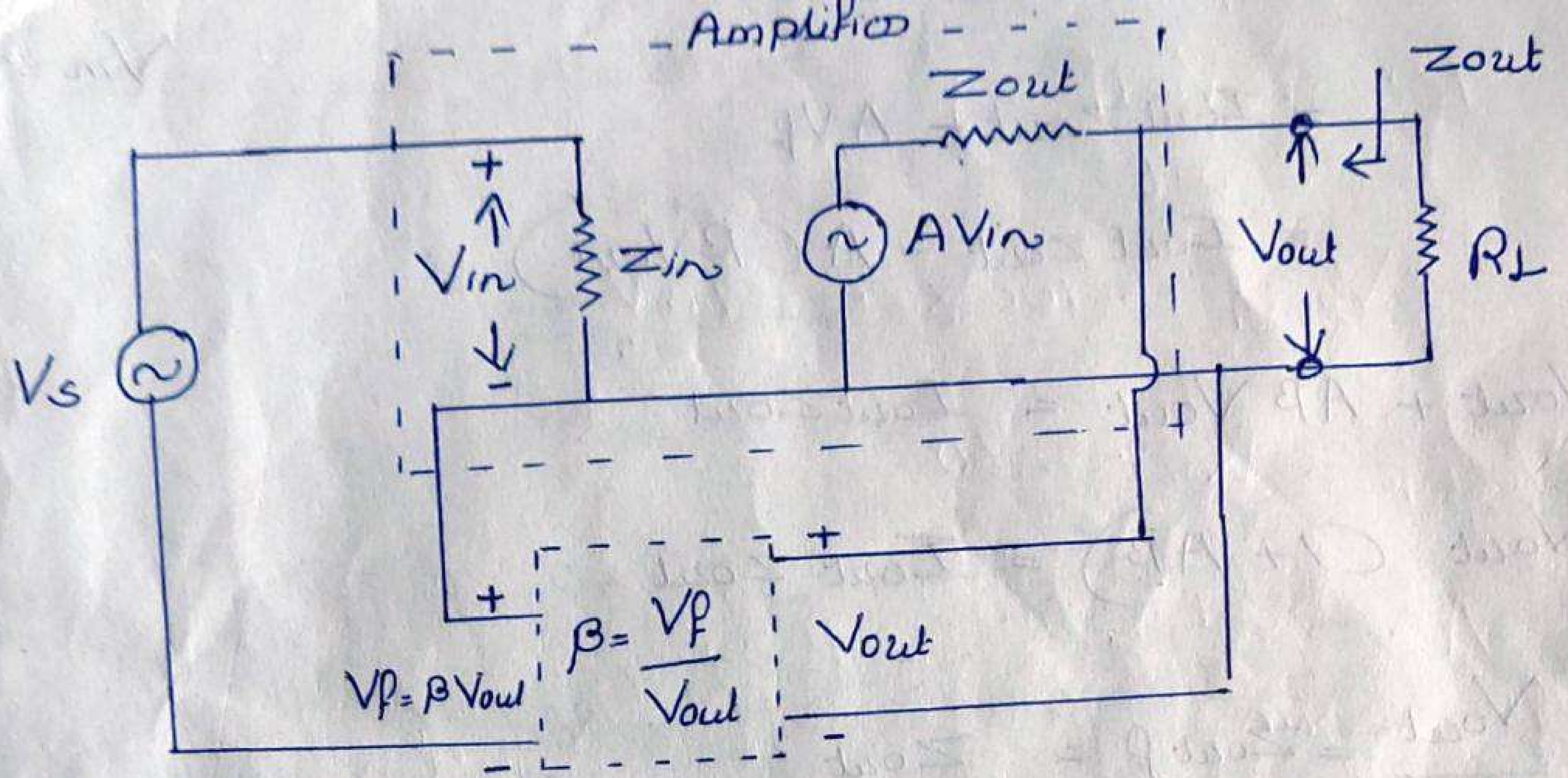
5) Reduced the o/p impedance

The o/p impedance of amplifier with negative fb is reduced by a factor $(1+A\beta)$

	Voltage Series	Voltage Shunt	Current Series	Current Shunt
Voltage gain	↓	↓	↓	↓
Noise	↓	↓	↓	↓
i/p impedance	↑	↓	↑	↓
o/p impedance	↓	↓	↑	↑
B.W	↑	↑	↑	↑

Effect of Negative Feedback On input impedance:

High i/p impedance is always desirable in an amplifier as it will not load preceding stage



$$I_{in} = \frac{V_{in}}{Z_{in}} = \frac{V_s - V_f}{Z_{in}}$$

$$= \frac{V_s - \beta V_{out}}{Z_{in}} = \frac{V_s - \beta A V_{in}}{Z_{in}}$$

$$I_{in} Z_{in} = V_s - \beta A V_{in}$$

$$\Rightarrow V_s = I_{in} Z_{in} + A\beta V_{in}$$

$$= I_{in} Z_{in} + A\beta I_{in} Z_{in}$$

$$= Z_{in} [I_{in}] \{1 + A\beta\}$$

$$\frac{V_s}{I_{in}} = Z_{in}(1 + A\beta)$$

$$Z_{inf} = Z_{in}(1 + A\beta)$$ $\Rightarrow$ Thus i/p impedance is increased by $(1 + A\beta)$

Effect of negative feedback on output impedance

The o/p impedance should be low.

$$V_{out} = I_{out} Z_{out} + AV_{in}$$

$V_{in} = -V_f$

$$= I_{out} Z_{out} - AV_f$$

$$= I_{out} Z_{out} - A(\beta V_{out})$$

$$V_{out} + A\beta V_{out} = I_{out} Z_{out}$$

$$V_{out}(1+A\beta) = I_{out} Z_{out}$$

$$\frac{V_{out}}{I_{out}} = Z_{out f} = \frac{Z_{out}}{(1+A\beta)}$$

$\Rightarrow$ o/p impedance is reduced by a factor $(1+A\beta)$

Effect of negative feedback on Bandwidth

The lower cut-off frequency is reduced & upper-cut off frequency is increased. Thus band-width is increased. The gain is reduced but it remain stable.

B.W with feed back = $(1+A\beta)$ B.W without feedback.

ampl
10
feedb
the

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An amplifier has an i/p impedance of 1kΩ & o/p imp 10 kΩ & a voltage gain of 10,000. If a negative feedback of $\beta = 0.02$ is applied to it, determine the i/p & o/p impedances of amplifier.

Open loop gain, $A = 10.000$

$\beta = 0.02$

$Z_{in} = 1K$

$Z_{out} = 10K$

$Z_{inf} = (1 + A\beta) Z_{in}$

$= (1 + 10{,}000 \times 0.02)\, 1 \times 10^3$

$= \underline{\underline{201\ k\Omega}}$

$Z_{outf} = \dfrac{Z_{out}}{1 + A\beta} = \dfrac{10K}{1 + 0.02 \times 10{,}000}$

$= \underline{\underline{49.75\Omega}}$

2. An amplifier with negative feedback has a voltage gain of 100. It is found that without feedback an i/p signal of 50 mV is required to produce a given o/p, whereas with feedback, the i/p signal must be 0.6 V for same o/p. Calculate A & β.

$A_f = 100$

$V_{in} = 50\ mV \qquad V_{out} = ?$

$V_{inf} = 0.6\ V \qquad V_{outf} = ?$

$V_{out} = V_{outf}$

$$A = \frac{V_{out}}{V_{in}} = \frac{V_{out}}{0.05}$$

EEE S_3 Module - III

Analog - Dhan

Mille

of

$$A_f = \frac{V_{out\,f}}{V_{in\,f}} = \frac{V_{out\,f}}{0.6}$$

$$100 = \frac{V_{out\,f}}{0.6}$$

$$V_{out\,f} = 100 \times 0.6 = \underline{\underline{60\,V}}$$

$$V_{out\,f} = V_{out} = 60$$

$$A = \frac{V_{out}}{V_{in}} = \frac{60}{0.05} = \underline{\underline{1200}}$$

$$A_f = \frac{A}{1 + A\beta}$$

$$100 = \frac{1200}{1 + 1200 \times \beta}$$

$$\underline{\underline{\beta = 9.16 \times 10^{-3}}}$$

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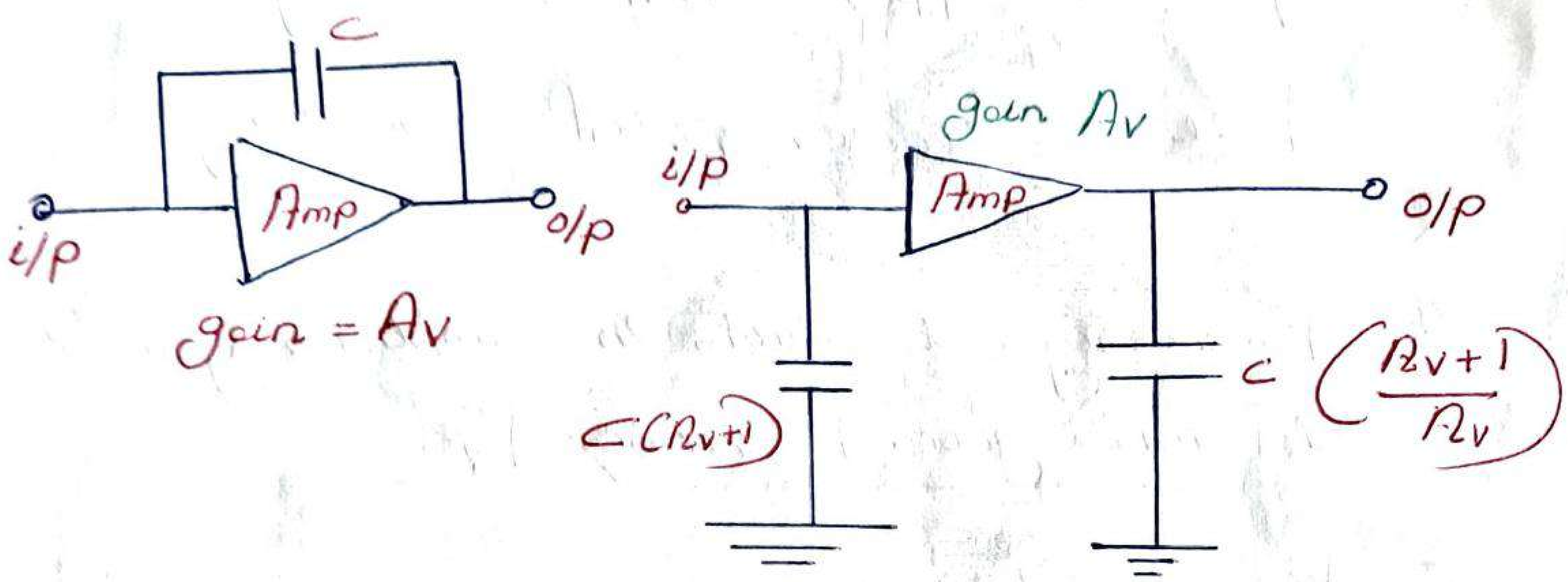
Miller's Theorem

During high frequencies, the internal capacitance of amplifier is important. The capacitance C_{bc} (base & collector) b/w i/p & o/p is shown



Millers theorem states that the capacitance C appears as the capacitance from i/p to gnd.

$$C_{in}\ (\text{miller}) = C\,(A_v+1)$$

It also states that the 'C' appears as the capacitance from o/p to gnd.

$$C_{out}\ (\text{miller}) = C\left(\frac{A_v+1}{A_v}\right)$$

Gain · Bandwidth Product

The product of voltage gain & bandwidth is always constant.

$$B \cdot W = f_{cu} - f_{cl}$$

$f_{cu} \Rightarrow$ upper cutoff frequency

$f_{cl} \Rightarrow$ lower cutoff frequency

The frequency at which the amplifier gain is 1 is called unity gain frequency f_T.

$$f_T = A_v \cdot B \cdot W$$

$A_v \Rightarrow$ midrange voltage gain.

1
32
2
35
4
6
17
11
21
33
28
10
37
18
45
41
39

Oscillators

Oscillator is a device used to generate oscillations without providing any i/p signals.

Oscillators

- Sinusoidal
- Non-Sinusoidal

1) RC oscillators
   a) RC Phase shift Oscillator
   b) Wein Bridge Oscillator
2) LC oscillators
   a) Hartley Oscillator
   b) Collpits Oscillator
3) Crystal Oscillators

1) RC-oscillators

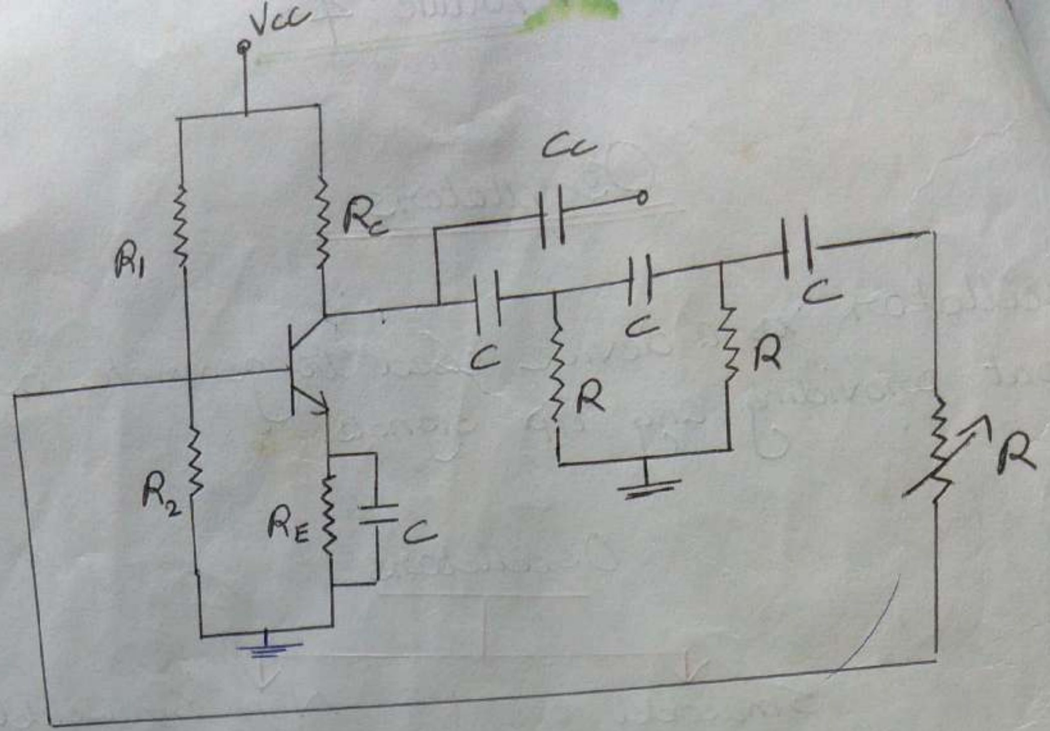
a) RC-phase shift Oscillator

Barkhausen Criterion ⇒ Basic Principle behind working of all oscillators.

1) $|A\beta| \geq 1$

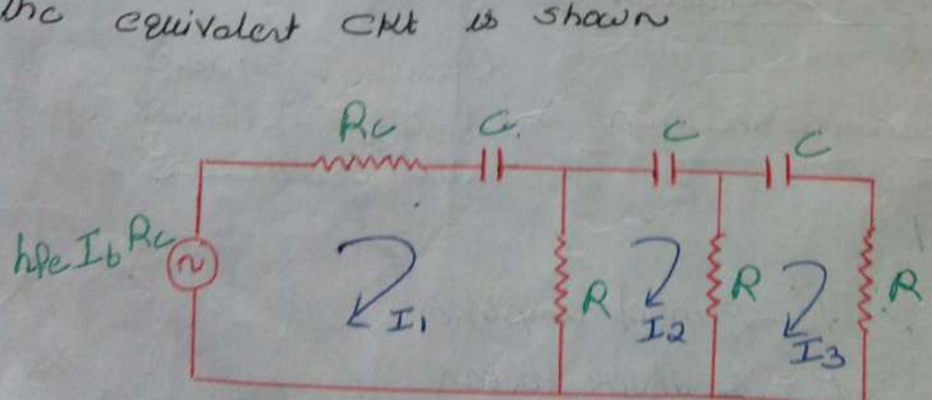
A = gain of amplifier
β = Feedback factor

2) Phase shift is $0°$ or $360°$



The circuit is set into oscillations by any random or variation caused in the base current, that may be either due to noise inherent in the transistor. This variation in base current is amplified in collector ckt. The o/p of the amplifier is supplied to an R-C feedback n/w. The RC-n/w produces a phase shift of 180° b/w o/p & i/p voltages. Since CE amplifier produces a phase reversal of i/p signal, total phase shift becomes 0° or 360°. The o/p of this n/w is thus in same phase as that of i/p.

The equivalent ckt is shown



$I_3 = I_b$

$$-R_C I_1 - \frac{1}{j\omega C} I_1 - R(I_1 - I_2) - h_{fe} I_b R_C = 0$$

$$+I_1\left(R_C + \frac{1}{j\omega C} + R\right) \mp R I_2 + h_{fe} I_b R_C = 0$$

Applying Kirchoffs voltage law

$$\left\{R + R_C + \frac{1}{j\omega C}\right\} I_1 - RI_2 + h_{fe} I_b R_C = 0 \quad \text{--- (1)}$$

$$-RI_1 + \left\{2R + \frac{1}{j\omega C}\right\} I_2 - RI_b = 0 \quad \text{--- (2)}$$

$$0 - RI_2 + \left\{2R + \frac{1}{j\omega C}\right\} I_b = 0 \quad \text{--- (3)}$$

$$\begin{vmatrix} R + R_C + \frac{1}{j\omega C} & -R & h_{fe} R_C \\ -R & 2R - jX_C & -R \\ 0 & -R & 2R - jX_C \end{vmatrix} = 0$$

$$\begin{vmatrix} R + R_C - jX_C & -R & h_{fe} R_C \\ -R & 2R - jX_C & -R \\ 0 & -R & 2R - jX_C \end{vmatrix} = 0$$

$$R + R_C - jX_C \left\{(2R - jX_C)^2 - R^2\right\} + R\left\{-R(2R - jX_C)\right\} + h_{fe} R_C R^2 = 0$$

$\Rightarrow$

Equating imaginary components

$$6R^2 X_C + 4RR_C X_C - X_C^3 = 0$$

$$\text{or} \quad X_C = \sqrt{6R^2 + 4RR_C}$$

$$2\pi fC = \frac{1}{\sqrt{6R^2 + 4RR_C}}$$

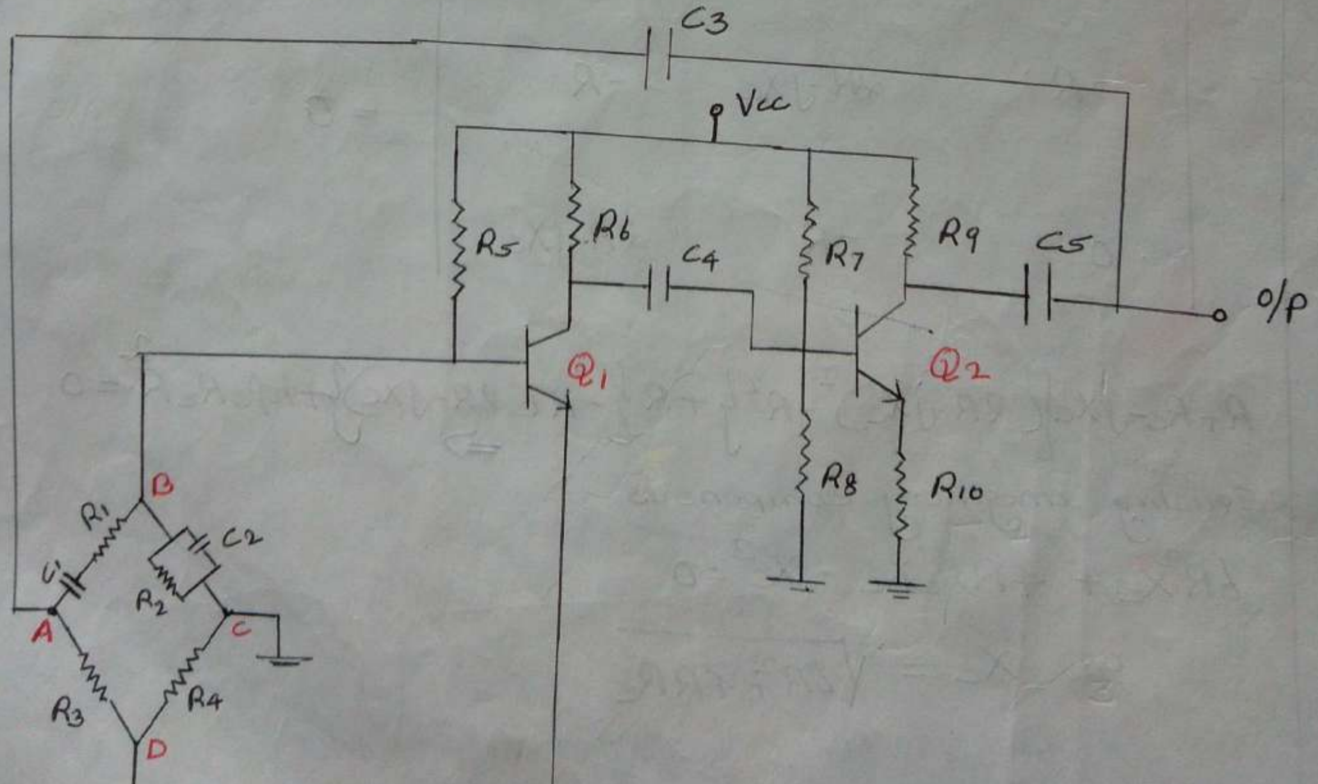
$$f = \frac{1}{2\pi C\sqrt{6R^2 + 4RR_C}}$$

$$f = \frac{1}{2\pi RC\sqrt{6 + \frac{4R_C}{R}}}$$

if $R = R_C$, then

$$f = \frac{1}{2\pi RC\sqrt{10}}$$

b) Wien Bridge Oscillator



The ckt diagram of Wien bridge oscillator is shown. It is essentially a two stage amplifier with R-C bridge (Wien bridge) ckt. If Wien bridge is not employed o/p of Q_2 is fedback directly to Q_1, this direct coupling will result in poor frequency stability. Thus by employing Wien bridge f.b n/w frequency stability is increased.

R_1 is in series with C_1, R_3, R_4 & R_2 parallel with C_2 forms 4 arms.

The bridge is balanced only when

$$R_3\left[\frac{R_2}{1+j\omega C_2R_2}\right] = R_4\left(R_1 - \frac{j}{\omega C_1}\right)$$

or

$$R_2R_3 = R_4(1+j\omega C_2R_2)(R_1 - j/\omega C_1)$$

$$R_2R_3 - R_4R_1 - \frac{C_2}{C_1}R_2R_4 + \frac{jR_4}{\omega C_1} - j\omega C_2R_2R_1R_4 = 0$$

Seperating real & imaginary terms

$$R_2R_3 - R_4R_1 - \frac{C_2}{C_1}R_2R_4 = 0$$

$$\text{or} \quad \frac{C_2}{C_1} = \frac{R_3}{R_4} - \frac{R_1}{R_2}$$

$$\& \quad \frac{R_4}{\omega C_1} - \omega C_2R_2R_1R_4 = 0$$

$$\text{or} \quad \omega^2 = \frac{1}{C_1C_2R_1R_2}$$

or

$$\omega = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}}$$

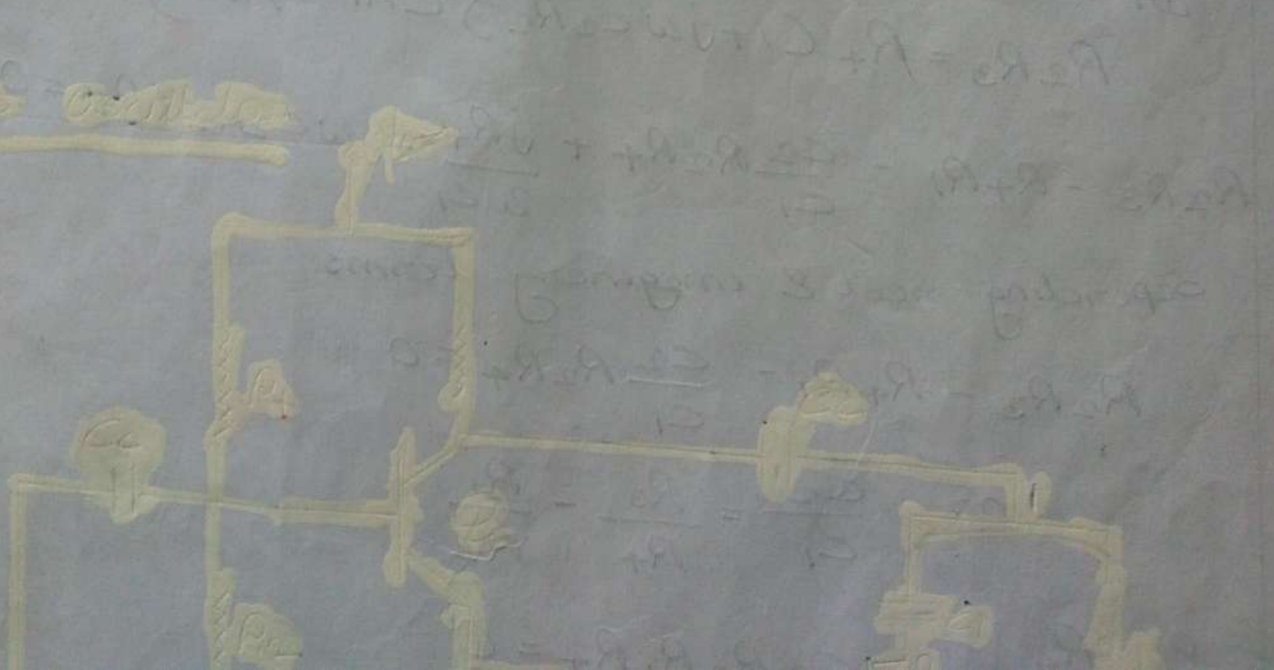
$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

if $C_1 = C_2 = C$ & $R_1 = R_2 = R$, then

$$f = \frac{1}{2\pi CR} \quad \& \quad R_3 = 2R_4$$

Thus in bridge ckt o/p will be in phase with i/p, only when bridge is balanced. So this bridge ckt can be used as feedback n/w for an oscillator, provided that the phase shift through amplifier is zero.

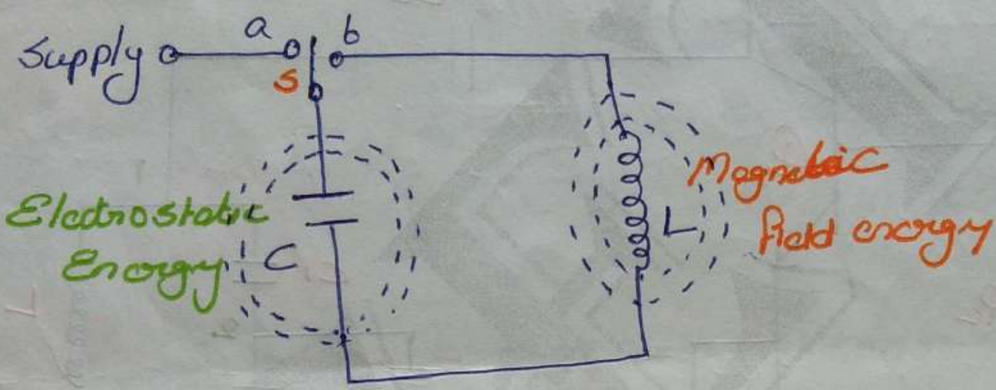
The o/p of second stage is supplied back to f.b n/w & Voltage across parallel combination R_2C_2 is fed to i/p of first stage. Q_1 act as oscillator & amplifier, Q_2 act as inverter to cause a phase shift of $180°$.



L-C oscillators

LC oscillators are used for high frequency generation. Hartley & colpitts oscillators are two practically used LC oscillators.

The basic component of two L-C oscillator is a tank circuit.

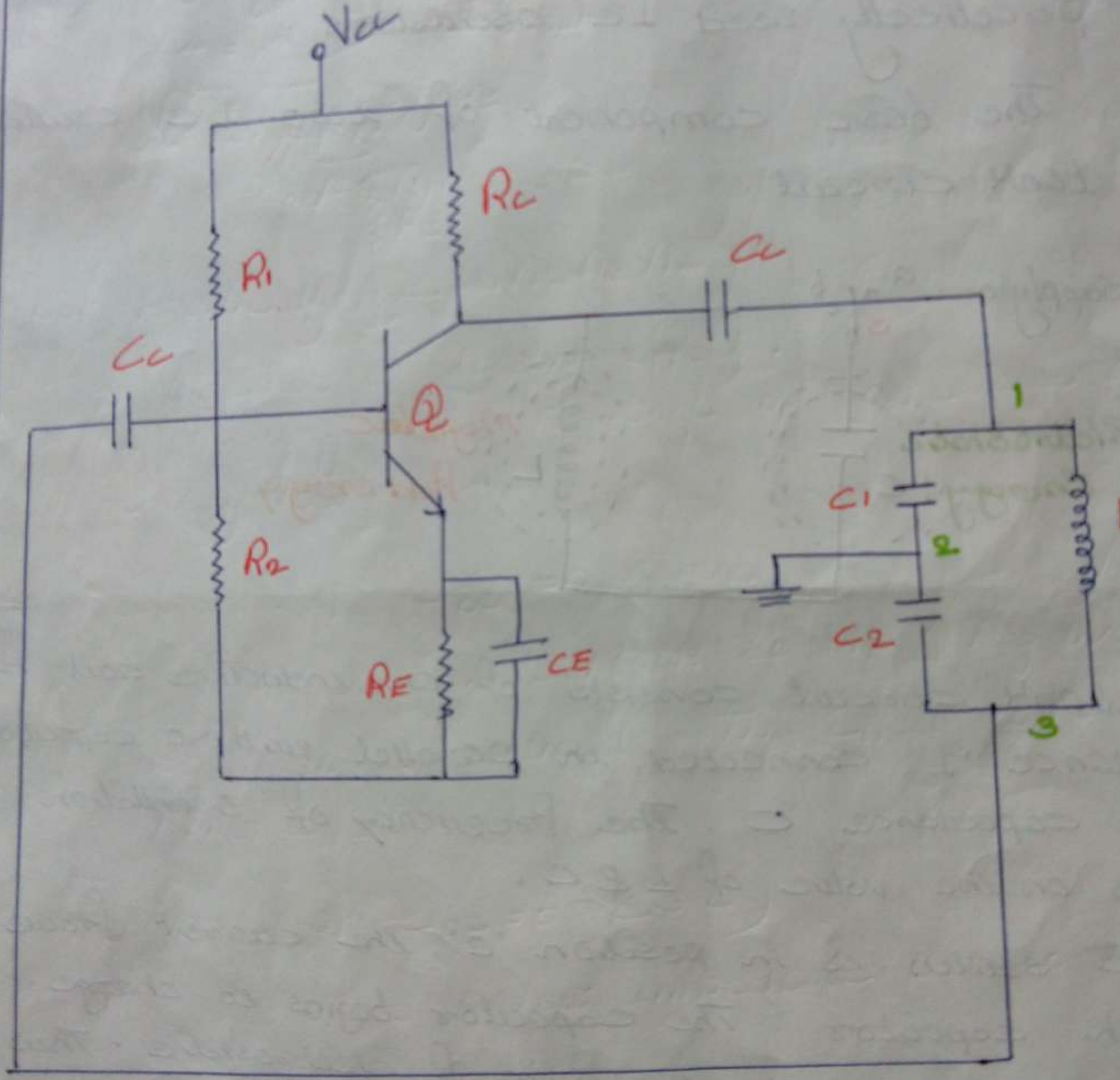


The tank circuit consists of an inductive coil having inductance 'L' connected in parallel with a capacitor having capacitance 'C'. The frequency of oscillation depends on the value of L & C.

If the switch is in position 'a', the current flows through capacitor. The capacitor begins to charge. It stores energy in the form of electrostatic. Thus there is electrostatic energy around the capacitor. When the capacitor is fully charged, it begins to discharge, ie, switch will be in position 'b'. Then current begins to flow (or the capacitor discharges) through inductor. The inductor now stores energy in the form of magnetic field.

Thus in tank ckt the electrostatic energy converted into magnetic field energy & vice versa. This will create oscillations.

Colpitt's Oscillator



oscillator ckt has an amplifier, & a tank circuit. The tank ckt has two capacitors $C_1 - C_2$ in parallel with an inductor L. The o/p of tank ckt is fed back to i/p through coupling capacitor. Transistor itself produces a phase shift of 180° & another phase shift of 180° is provided by capacitive feed back. Thus a total phase shift of 360° is obtained.

When Vcc is given, C_1 & C_2 are charged. These C_1 & C_2 discharge through L, setting up oscillations of frequency $f = \frac{1}{2\pi}\sqrt{\frac{1}{LC_1}+\frac{1}{LC_2}}$. The oscillations across C_2 are applied to amplifier section.

$$\beta = \frac{C_1}{C_2}$$

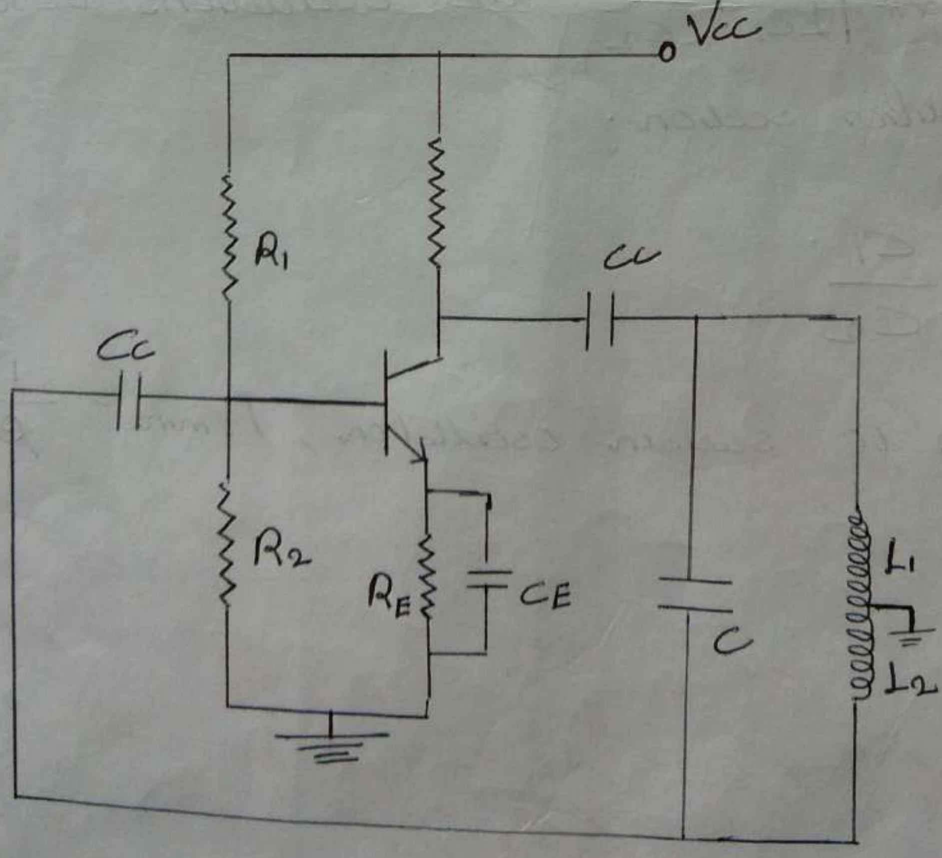
Minimum gain to sustain oscillation, $A_{min} = \frac{1}{\beta}$.

Hartley Oscillator

Hartley Oscillator ckt is similar to Colpitts except that phase shift n/w consists of two inductors L_1 & L_2 & capacitor C, instead of two capacitors & one inductor. The operation of ckt is similar to Colpitt's Oscillator.

Frequency of Oscillation

$$f = \frac{1}{2\pi\sqrt{[C(L_1+L_2+2M)]}}$$

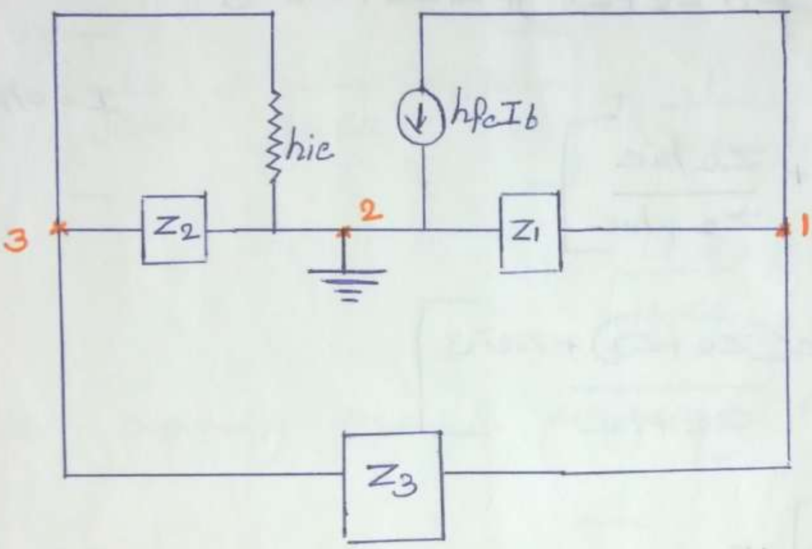


Q8) Derivation of Oscillator Frequency of Colpitts & Hartley Oscillator

(10 marks)

The hybrid equivalent model is drawn with following assumptions.

* h_{re} is small, ∴ $h_{re}V_{out}$ is negligible.
* h_{oe} is small, ∴ $\frac{1}{h_{oe}}$ is omitted



The load impedance b/w o/p terminals

$$Z_L = Z_1 \parallel \left[Z_3 + (Z_2 \parallel h_{ie})\right]$$

$$= Z_1 \parallel \left[Z_3 + \frac{Z_2 h_{ie}}{Z_2 + h_{ie}}\right]$$

$$= Z_1 \parallel \left[\frac{Z_3(Z_2 + h_{ie}) + Z_2 h_{ie}}{Z_2 + h_{ie}}\right]$$

$$= Z_1 \parallel \left[\frac{h_{ie}(Z_2 + Z_3) + Z_2 Z_3}{Z_2 + h_{ie}}\right]$$

$$\frac{1}{Z_L} = \frac{1}{Z_1} + \frac{Z_2 + h_{ie}}{h_{ie}(Z_2+Z_3)+Z_2Z_3}$$

$$= \frac{h_{ie}(Z_1+Z_2+Z_3)+Z_1Z_2+Z_2Z_3}{Z_1[h_{ie}(Z_2+Z_3)+Z_2Z_3]}$$

or

$$Z_L = \frac{Z_1[h_{ie}(Z_2+Z_3)+Z_2Z_3]}{h_{ie}(Z_1+Z_2+Z_3)+Z_1Z_2+Z_2Z_3} \quad \text{— (a)}$$

I = o/p current

$$V_{out} = I\left[Z_3 + \frac{Z_2 h_{ie}}{Z_2+h_{ie}}\right]$$

$$= I\left[\frac{h_{ie}(Z_2+Z_3)+Z_2Z_3}{Z_2+h_{ie}}\right]$$

$$V_f = \left[\frac{Z_2 h_{ie}}{Z_2+h_{ie}}\right] I$$

$$\beta = \frac{V_f}{V_{out}} = \frac{Z_2 h_{ie}}{h_{ie}(Z_2+Z_3)+Z_2Z_3}$$

For oscillators $A\beta = 1$

A for CE amplifier $= \frac{-h_{fe}}{h_{ie}} Z_L$

$A\beta = 1$

$$\Rightarrow \frac{-h_{fe}}{h_{ie}} Z_L \times \frac{Z_2 h_{ie}}{h_{ie}(Z_2+Z_3)+Z_2Z_3} = 1 \quad \text{— (1)}$$

Substitute the value of Z_L in (2) in (1)
& after rearranging we have

$$h_{ie}(Z_1+Z_2+Z_3)+Z_1Z_2(1+h_{fe})+Z_2Z_3=0 \quad (4)$$

The above is the general equation for LC oscillator

* For colpitts.

$$Z_1=\frac{1}{j\omega C_1},\quad Z_2=\frac{1}{j\omega C_2},\quad Z_3=j\omega L$$

substitute Z_1, Z_2 & Z_3 in Eqn (2)

$$h_{ie}\left[\frac{1}{j\omega C_1}+\frac{1}{j\omega C_2}+j\omega L\right]+\frac{1}{j\omega C_1}\times\frac{1}{j\omega C_2}(1+h_{fe})$$

$$+\frac{1}{j\omega C_2}\times j\omega L=0$$

After seperating real & imaginary parts $\left\{\frac{1}{j}=-j\right.$

$$-j\,h_{ie}\left[\frac{1}{\omega C_1}+\frac{1}{\omega C_2}-\omega L\right]-\frac{1+h_{fe}}{\omega^2C_1C_2}+\frac{L}{C_2}=0$$

Equating imaginary part to zero

$$h_{ie}\left[\frac{1}{\omega C_1}+\frac{1}{\omega C_2}-\omega L\right]=0$$

$$\frac{1}{\omega C_1}+\frac{1}{\omega C_2}=\omega L$$

$$\frac{C_1+C_2}{\omega C_1C_2}=\omega L \quad \text{or} \quad \omega^2=\frac{C_1+C_2}{LC_1C_2}$$

$$\omega=\sqrt{\frac{C_1+C_2}{LC_1C_2}}=\sqrt{\frac{1}{LC_1}+\frac{1}{LC_2}}$$

or $$f = \frac{1}{2\pi}\sqrt{\frac{1}{LC_1} + \frac{1}{LC_2}}$$

* For Hartley

$$Z_1 = j\omega(L_1+M) \quad Z_2 = j\omega(L_2+M), \quad Z_3 = \frac{1}{j\omega C}$$

Substitute Z_1, Z_2 & Z_3 in Equ (2)

& Equating imaginary parts to zero

$Z_1 = j\omega(L_1+M)$

$Z_2 = j\omega(L_2+M)$

$Z_3 = \frac{1}{j\omega C}$

$$\omega j\left[L_1 + L_2 + 2M - \frac{1}{\omega^2 C}\right] = 0$$

$$L_1 + L_2 + 2M = \frac{1}{\omega^2 C}$$

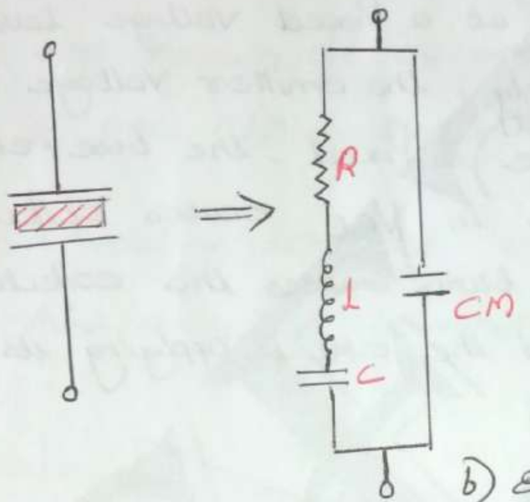
$$C\omega^2 = \frac{1}{L_1 + L_2 + 2M}, \quad \omega = \frac{1}{\sqrt{C(L_1 + L_2 + 2M)}}$$

$$\omega = 2\pi f$$

$$\therefore f = \frac{\omega}{2\pi} = \frac{1}{2\pi\sqrt{C(L_1 + L_2 + 2M)}}$$

29) 3) Crystal Oscillators (5 marks)

A quartz crystal exhibits a very important property known as piezo-electric effect. When a mechanical pressure is applied across the faces of the crystal, a voltage proportional to mechanical pressure appears across the crystal & vice versa



a) Crystal

b) Electrical Equivalent ckt of Crystal.

The crystal actually behaves as a series RLC ckt in parallel with Cm. The crystal has two resonant frequencies.

⇒ Series resonance frequency f_s at which, $2\pi f L = \frac{1}{2\pi f C}$ & in this case crystal impedance is low.

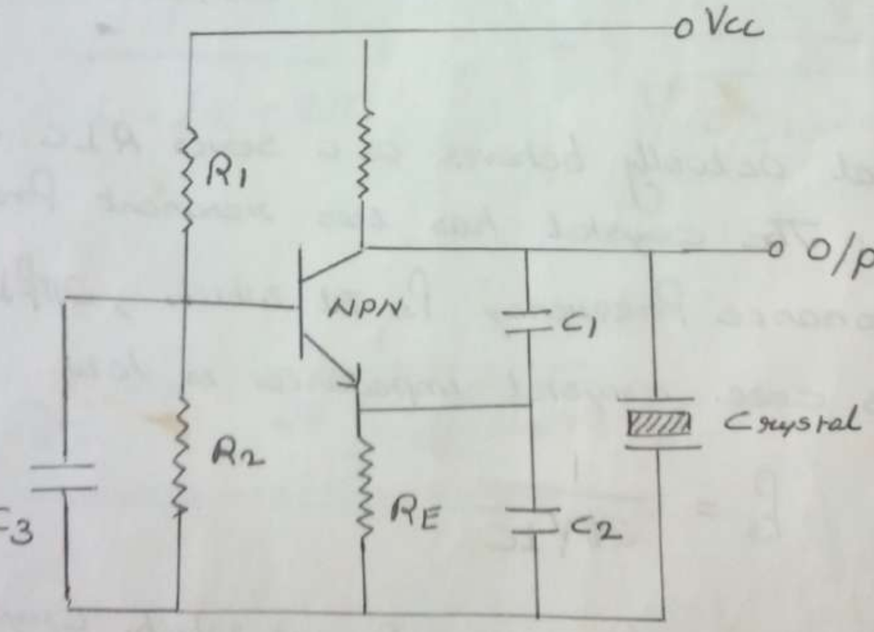
$$f_s = \frac{1}{2\pi\sqrt{LC}}$$

⇒ Parallel resonance frequency f_P, at which crystal impedance is high

$$f_P = \frac{1}{2\pi}\sqrt{\frac{1+C/C_m}{LC}}$$

To stabilize the frequency of oscillator, a crystal must be operated at either its series or parallel resonant frequency

Since parallel resonant impedance of crystal is maximum, it is connected in parallel. C_1 & C_2 form a capacitor voltage divider which returns a portion of o/p voltage to the transistor emitter. Capacitor C_3 provides an ac short ckt across R_2 to ensure that the transistor base remains at a fixed voltage level. As the o/p voltage increases positively, the emitter voltage also increases & since the base voltage is fixed, the base-emitter voltage is reduced. The reduction in V_{BE} causes collector current I_C to diminish, & this in turn causes the collector voltage V_C to increase positively. Thus the ckt is applying its own i/p & a state of oscillation exist.



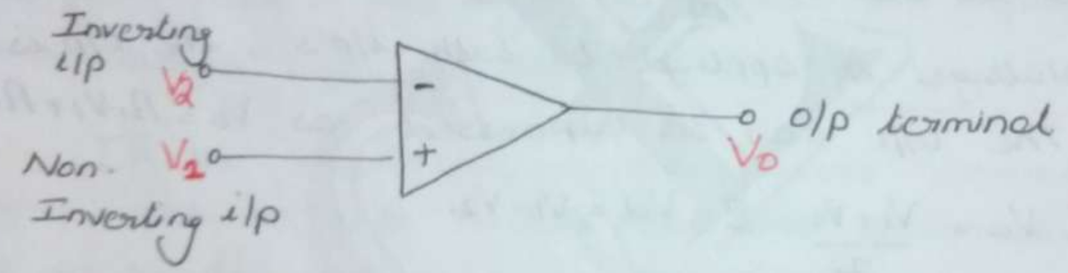
Operational Amplifier

The op-amp is a multiterminal device which internally is quite complex. The Op-amp's performance can be completely described by its terminal characteristics & those of external components that are connected to it.

The ckt diagram of op-amp is shown. It has two i/p terminals & one o/p terminal

-Ve ⇒ Inverting terminal

+Ve ⇒ Non inverting terminal



Consider the op-amp shown in fig. This op-amp is said to be ideal if it has following characteristics

1) Open loop voltage gain, $A_{OL} = \infty$
2) Input impedance, $R_i = \infty$
3) o/p impedance, $R_0 = 0$
4) Bandwidth $= \infty$
5) Zero offset ie, $V_0 = 0$ when $V_1 = V_2 = 0$

The op-amp amplifies the diff. i/p $V_d = V_1 - V_2$.

Characteristics of OP-amp.

1) Common Mode Configuration

In the case of ideal op-amp, when the two i/p's are equal, there is no o/p voltage. In practical case, the o/p voltage depends not only upon the diff signal V_d, but it also depends upon the avg of i/p signal called the common-mode signal, $V_c = \frac{V_1 + V_2}{2}$

For the differential amplifier, though the ckt is symmetric, but because of the mismatch, the gain at the o/p w.r.t the positive terminal is slightly different in magnitude to that of negative terminal. So even when the same voltage is applied to both i/p's, the o/p is not zero. The o/p can be expressed as $V_0 = A_1 V_1 + A_2 V_2$ —(1)

Since, $V_c = \frac{V_1 + V_2}{2}$ & $V_d = V_1 - V_2$

$$V_1 = V_c + \frac{V_d}{2}$$

$$V_2 = V_c - \frac{V_d}{2}$$

Substituting V_1 & V_2 in (1)

$$V_0 = A_d V_d + A_c V_c$$

where $A_d = \frac{1}{2}(A_1 - A_2)$

$A_c = A_1 + A_2$

$A_d \Rightarrow$ Voltage gain for diff signal

$A_c \Rightarrow$ Voltage gain for common mode signal.

The common mode voltage gain, $A_{cm} = \frac{V_0}{V_1 + V_2}$

Common Mode Rejection Ratio (CMRR) is defined as ratio of differential voltage gain to common mode voltage gain.

$$CMRR = \frac{A_d}{A_{cm}}$$

The value of A_{cm} is very small compared to A_d.
∴ CMRR is very large.

Higher the value of CMRR, better is the matching b/w 2 i/p's terminals & smaller is the o/p common-mode voltage. Thus it has a better ability to reject common mode voltages such as noise

If an undesirable signal appears common to both i/p's such as both noise, then the external to which it get rejected depends upon the CMRR

2) Large Signal Voltage Gain

Since the op-amp, amplifies difference voltage b/w two i/p terminals, the voltage gain of the amplifier is defined as

$$\text{Voltage gain} = \frac{\text{o/p Voltage}}{\text{differential i/p}}$$

$$A = V_o / V_{id}$$

Since the o/p signal amplitude is much larger than i/p, the voltage gain is commonly called large signal Voltage gain.

3) Slew Rate (SR)

It is defined as the maximum rate of change of o/p Voltage per unit of time

$$S.R = \frac{dV_o}{dt} \ V/\mu sec \quad = 2\pi f_m V_m$$

⇒ The S.R indicates how rapidly the o/p of an op-amp can changes in response to change in i/p frequency.

⇒ SR is one of the imp. factor in selecting the op-amp for ac application, particularly at relatively high frequency

SR of IC741 = 0.5V/μsec

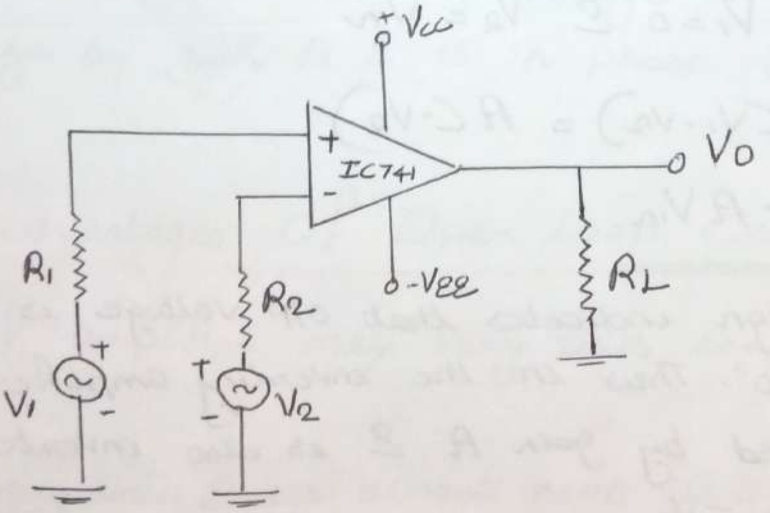
Op-Amp Configuration

- Open Loop Configuration (∵ no feedback)
  - Differential
  - Inverting
  - Non Inverting
- Closed loop Configuration (Feedback is given)
  - Differential
  - Inverting
  - Non Inverting.

Open loop configuration

In the open loop configuration of op-amp, there is no connection exists b/w o/p & i/p terminals, i.e the o/p signal is not feedback in any form as part of i/p signal.

1) Differential Amplifier

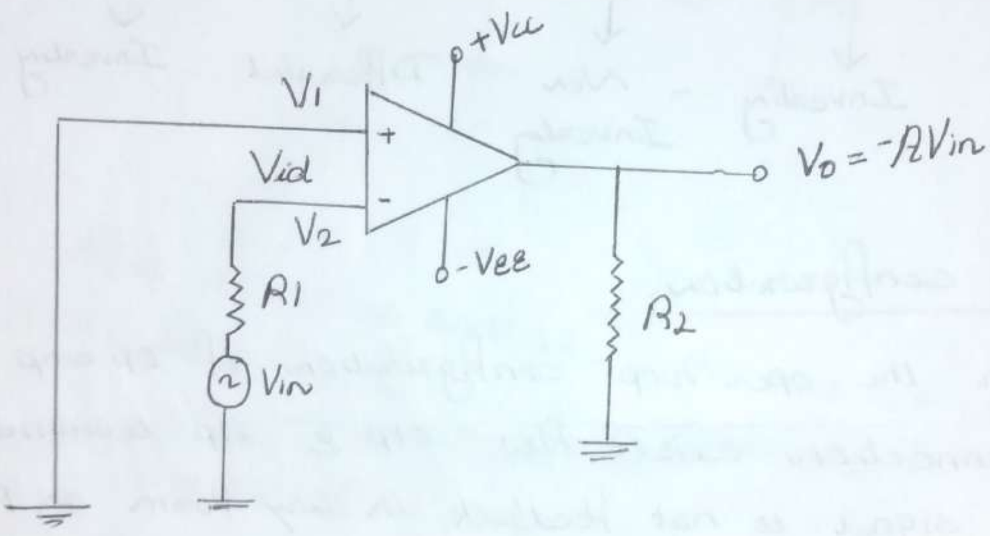


Here V_1 & V_2 are applied to +Ve & -Ve i/p terminals. Since the op-amp amplifies the diff b/w two i/p signals, the configuration is called differential amplifier

$$\text{o/p Voltage, } V_o = A(V_1 - V_2) = A V_{id}$$

$$\text{Open loop gain, } A = \frac{V_o}{V_1 - V_2} = \frac{V_o}{V_{id}}$$

2) Inverting Amplifier



Only one i/p is applied ie, to the inverting i/p terminal. The non-inverting i/p terminal is grounded.

$$\text{Since } V_1 = 0 \text{ \& } V_2 = V_{in}$$

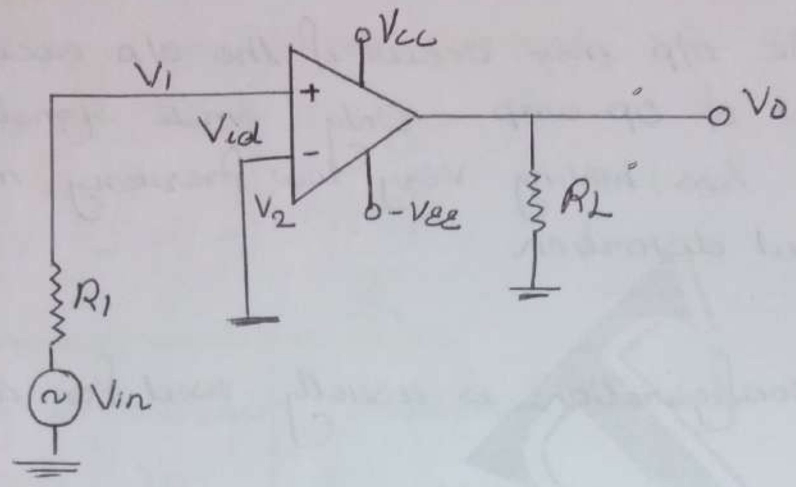
$$V_o = A(V_1 - V_2) = A(-V_2)$$

$$V_o = -A V_{in}$$

The negative sign indicates that o/p Voltage is out of phase w.r.t i/p by 180°. Thus in the inverting amplifier the i/p signal is amplified by gain A & is also inverted at o/p

$$\text{ie, } A = \frac{-V_o}{V_{in}}$$

3) Non-Inverting Amplifier



Here the i/p is applied to the non-inverting i/p terminal & the inverting terminal is grounded.

$$V_1 = V_{in} \quad \& \quad V_2 = 0$$

$$V_o = A(V_1 - V_2) = AV_{in}$$

$$A = V_o / V_{in}.$$

This means that the o/p voltage is larger than the i/p voltage by gain A & is in phase with the i/p signal.

Disadvantages Of Open Loop Configuration

1) Gain of amplifier may vary with temp & saturation voltages

2) B.W is very small & its almost zero. B.W refers to the range of frequencies over which the gain will remain constant

3) Open loop gain of op-amp is very high. So the o/p is either +Ve or -Ve saturation or switches b/w +Ve or -Ve saturation voltages. So open loop configuration is not used for linear application.

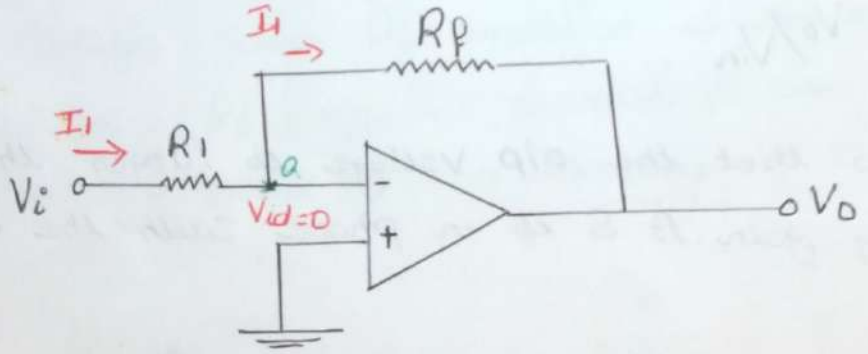
4) Clipping of the o/p may occur if the o/p exceeds the saturation level of op-amp. Only small signals of the order of µV or less, having very low frequency may be amplified without distortion

5) Open-loop configuration is usually used for non-linear applications.

Closed Loop Op-amp Configurations

⇒ there is fb from o/p to i/p.

1) The Inverting Amplifier



The o/p voltage V_o is fb to the inverting i/p terminal through R_f - R_1 n/w, where R_f is the feedback resistor. i/p signal V_i is applied to inverting i/p terminal through R_1 & non inverting i/p terminal of op-amp is grounded.

For simplicity, assume ideal op-amp

As $V_{id} = 0$, node 'a' at ground potential &

$$I_1 = \frac{V_i}{R_1}$$

Since op-amp draws no current, all current flowing through ~~Rf~~ R_1, flows through R_f

$$V_o = -I_1 R_f = \frac{-V_i R_f}{R_1}$$

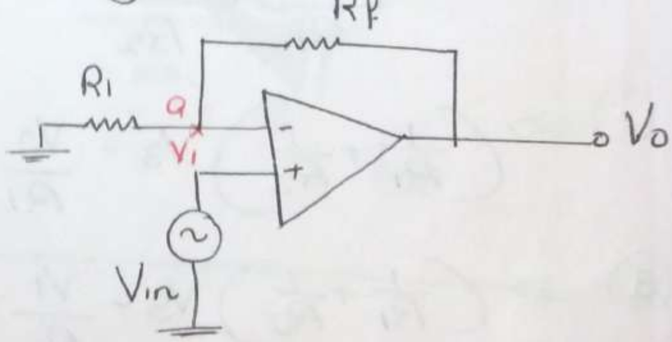
Hence gain of inverting amplifier (closed loop) is

$$A_{CL} = \frac{V_o}{V_i} = \frac{-R_f}{R_1}$$

The negative sign indicates a phase shift of 180° b/w V_i & V_o.

2) Non Inverting Amplifier

Voltage series f.b amplifier is also known as non-inverting f.b amplifier because it uses f.b & the i/p signal is applied to non-inverting i/p terminal of op-amp.



As the $V_{id} = 0$,

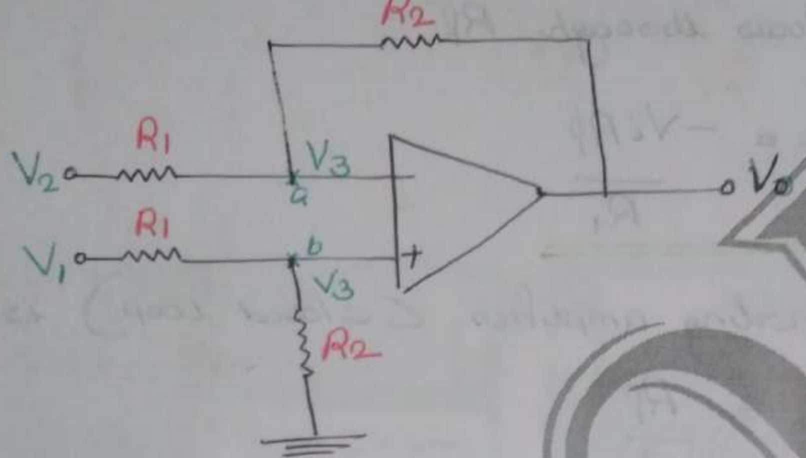
$$V_1 = V_{in}$$

$$V_1 = \frac{V_o R_1}{R_1 + R_f}$$

Closed loop voltage gain, $A_{CL} = \frac{V_o}{V_{in}} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}$

3) Differential Amplifier

This amplifier amplifies the diff b/w two signals



Since the differential voltage at i/p is zero 'a' & 'b' are at same potential, ie V_3

The nodal equation at 'a' is

$$\frac{V_3 - V_2}{R_1} + \frac{V_3 - V_0}{R_2} = 0 \quad (1)$$

The nodal equation at 'b' is

$$\frac{V_3 - V_1}{R_1} + \frac{V_3}{R_2} = 0 \quad (2)$$

(1) $\Rightarrow \left(\frac{1}{R_1} + \frac{1}{R_2}\right) V_3 - \frac{V_2}{R_1} = \frac{V_0}{R_2} \quad (3)$

(2) $\Rightarrow \left(\frac{1}{R_1} + \frac{1}{R_2}\right) V_3 - \frac{V_1}{R_1} = 0 \quad (4)$

(3) - (4) $\quad \frac{1}{R_1}(V_1 - V_2) = \frac{V_0}{R_2}$

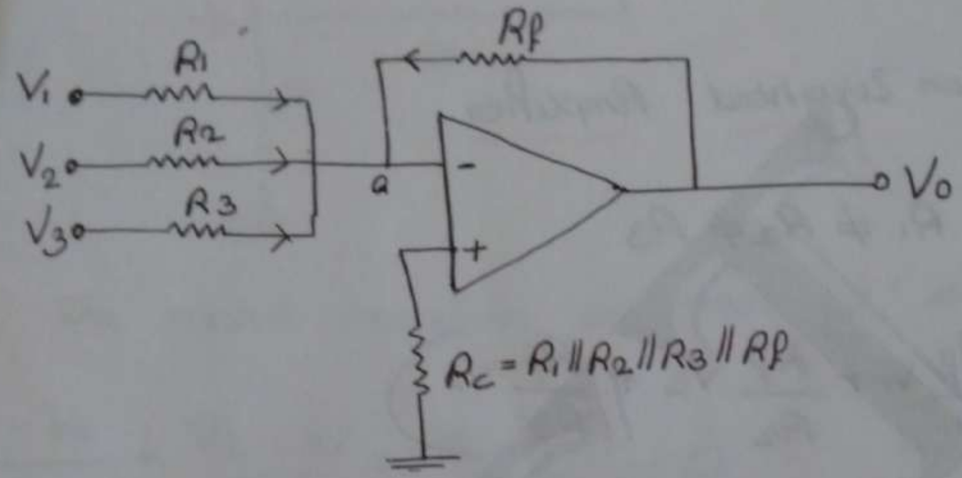
$$V_0 = \frac{R_2}{R_1}(V_1 - V_2)$$

Such a ckt is very useful in detecting very small differences in signals.

Summing Amplifier

Op amp may be used to design a ckt whose o/p is the sum of several i/p signals. Such a ckt is called summing amplifier or a summer. The most useful application of op-amp is analog computer. This ckt can be used to add a dc signal or an ac signal. This ckt will produce an o/p voltage which is proportional to or equal to algebraic sum of all i/p voltage & each multiplied by a constant gain factor.

(2) Inverting Summing Amplifier



The inverting configuration consists of 3 i/p voltages V_1, V_2 & V_3. 3 i/p resistors R_1, R_2, R_3 & R_f. Assuming that the op-amp is ideal one (ie, $A_{OL} = \alpha$ & $R_I = \alpha$ & $I_B = 0$). Since the i/p bias current is assumed to be zero there is no voltage drop across R_C & hence the non-inverting i/p terminal is at ground potential.

The voltage at node 'a' is zero as the non-inverting i/p terminal is grounded. The nodal equation by KCL at node 'a' is

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_o}{R_f} = 0$$

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right) \quad \text{--- (1)}$$

⇒ Summing Amplifier

when $R_1 = R_2 = R_3 = R$, equ (1) becomes

$$V_0 = \frac{-R_f}{R}(V_1 + V_2 + V_3)$$

⇒ Scaling or Weighted Amplifier

when $R_1 \neq R_2 \neq R_3$

$$V_0 = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

⇒ Average ckt

Let 'n' be no: of inputs

when $R_1 = R_2 = R_3 = R$

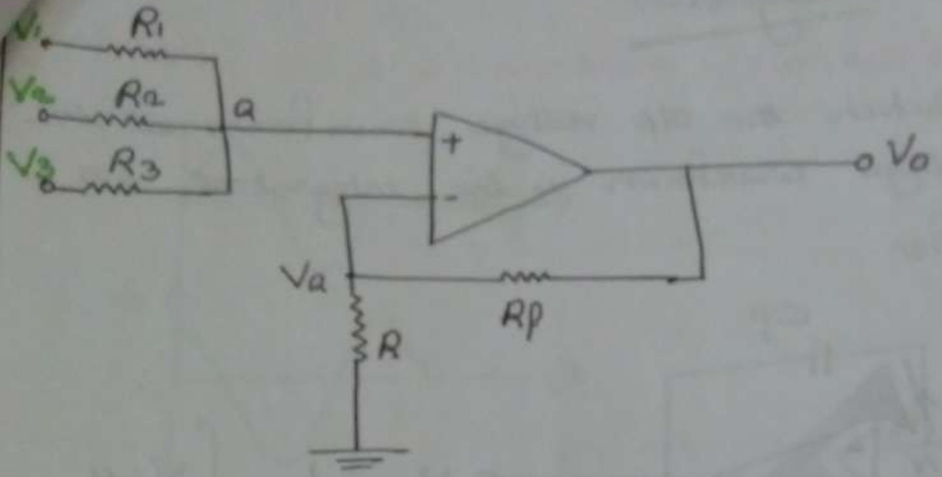
$$\frac{R_f}{R} = \frac{1}{n}$$

For eg: for 3 i/p's

$$V_0 = \frac{-1}{3}(V_1 + V_2 + V_3)$$

b) Non - Inverting Summing Amplifier

A summer that gives a non inverted sum is the non inverting summing amplifier.



The nodal equation at node 'a' is

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

$$V_a = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

The op-amp & two resistors R_f & R constitute a non-inverting amplifier with

$$V_o = \left(1 + \frac{R_f}{R}\right) V_a$$

∴ o/p voltage is

$$V_o = \left(1 + \frac{R_f}{R}\right) \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

which is a non-inverted weighted sum of i/p's

Let $R_1 = R_2 = R_3 = R = R_f/2$

then $V_o = V_1 + V_2 + V_3$

Instrumentation Amplifier

Instrumentation amplifiers are used in monitoring & controlling of physical quantities, in the industrial process for the measurement & control of temperature, humidity & light intensity. A transducer can convert one form of energy into another is used to sense & deliver the required information in the form of electrical quantity.

The major function of an instrumentation amplifier is precise amplification of low level o/p. signal of transducer.

Commonly used instrumentation amplifier are

→ AD 521, AD 524

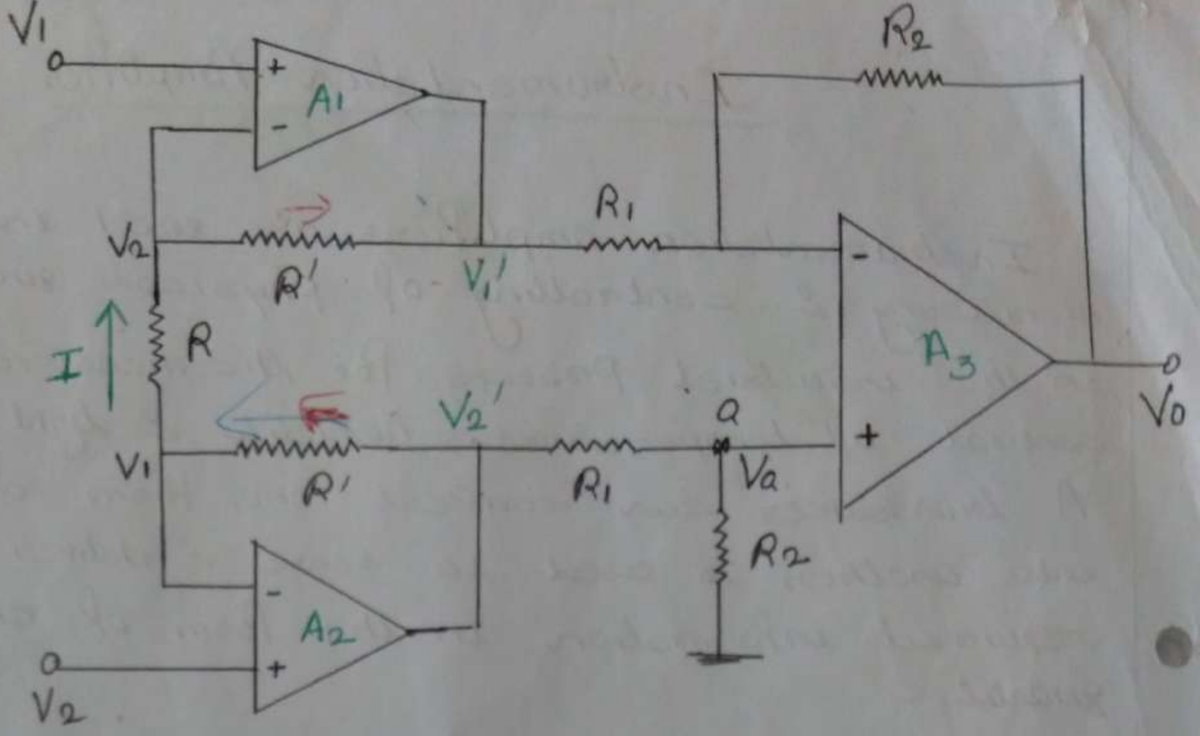
Features

1) high gain accuracy

2) high CMRR

3) high gain stability

4) Low o/p impedance.



A_1 & A_2 are Voltage follower or buffer ckts acting as i/p stage for each of i/p's V_1 & V_2.

Let $\underline{V_1 = V_2}$ $\Rightarrow$ The voltage across R is zero. Since no currents flows through R & R'. $V_1 = V_1'$ & $V_2 = V_2'$

If $\underline{V_1 \neq V_2}$ $\Rightarrow$ Then current flows throug R

$$I = \frac{V_1 - V_2}{R}.$$

The Voltage at node a

$$V_a = \frac{V_2' R_2}{R_1 + R_2}$$

By superposition theorem $V_0 = \frac{-R_2}{R_1} V_1' + \left[1 + \frac{R_2}{R_1}\right] \frac{R_2 V_2'}{R_1 + R_2}$ $\rightarrow$ (1)

Let $R_1 \gg R_2$

Equ (1) $\Rightarrow V_0 = +\frac{R_2}{R_1}(V_2' - V_1') \longrightarrow (2)$

$V_1' = V_1 + IR'$

$V_2' = V_2 - IR'$

Substitute V_1' & V_2' in Equ (2)

$$V_0 = \frac{R_2}{R_1}\left[V_2 - V_1 - 2IR'\right] \longrightarrow (3)$$

$I = \frac{V_1 - V_2}{R}$ in Equ (3)

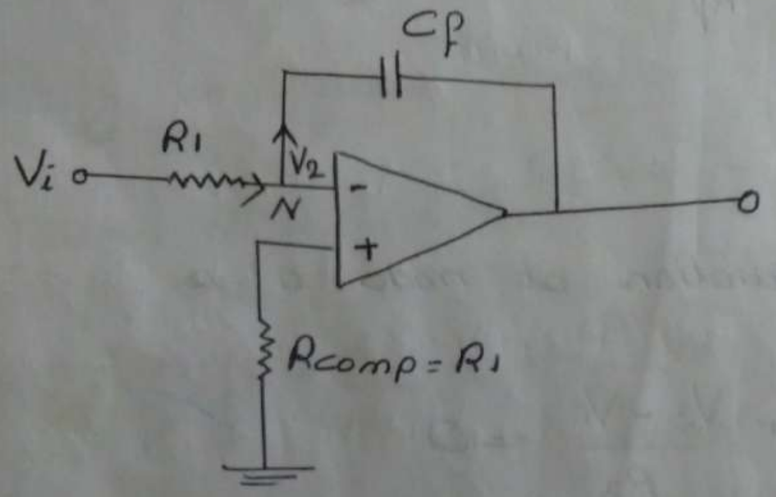
$$V_0 = \frac{R_2}{R_1}\left[V_2 - V_1 - 2R'\left(\frac{V_1 - V_2}{R}\right)\right]$$

$$= \frac{R_2}{R_1}\left[V_2 - V_1 - \frac{2R'}{R}V_1 + \frac{2R'}{R}V_2\right]$$

$$V_0 = \frac{R_2}{R_1}\left[1 + \frac{2R'}{R}\right](V_2 - V_1)$$

Integrator

A ckt in which the o/p voltage waveform is the integral of i/p voltage waveform is the integrator or integrator amplifier



$V_0 = \frac{-1}{R_1 C_f} \int V_i dt$

The nodal equation at node 'N' is

$$\frac{V_i - V_2}{R_1} = C_f \frac{d}{dt}(V_2 - V_0)$$

$N \Rightarrow$ Virtual ground.

$$\frac{V_i}{R_1} = -C_f \frac{dV_0}{dt}$$

$$\frac{V_i}{R_1} = -C_f \frac{dV_0}{dt}$$

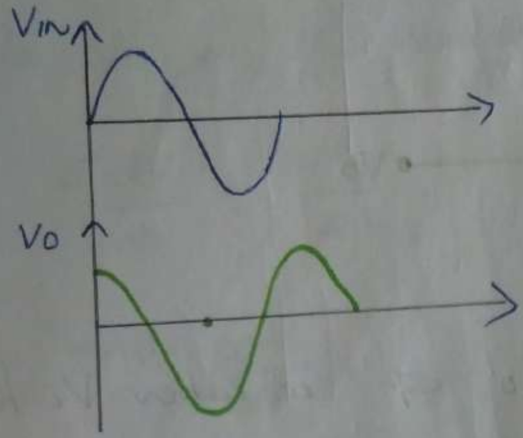
$$\frac{dV_0}{dt} = \frac{-V_i}{R_1 C_f}$$

$$\text{ie, } V_0 = \frac{-1}{R_1 C_f} \int V_i dt + C$$

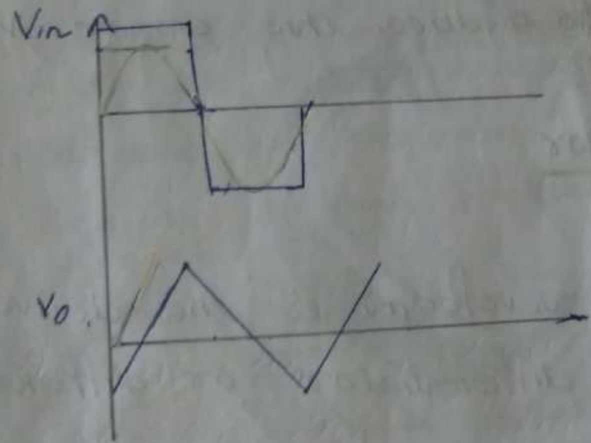
Thus the o/p is $-1/R_1 C_f$ times the integral of i/p.

$R_1 C_f$ = time const.

* If the i/p is a sinewave, o/p will be cosine

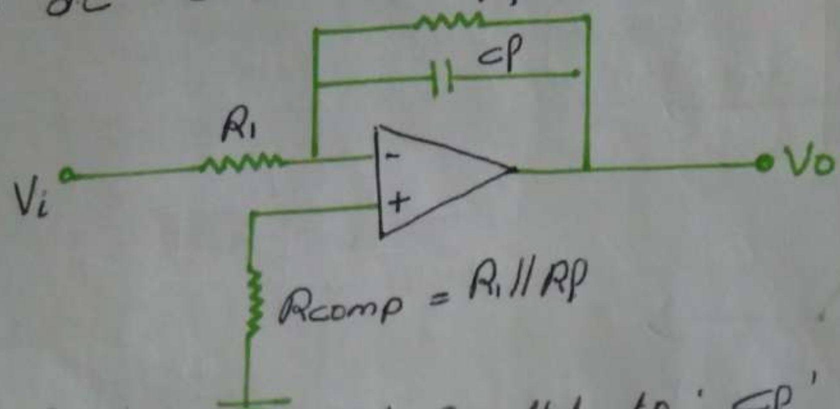


* If the i/p is a square wave, o/p is a triangular wave.



Practical Integrator

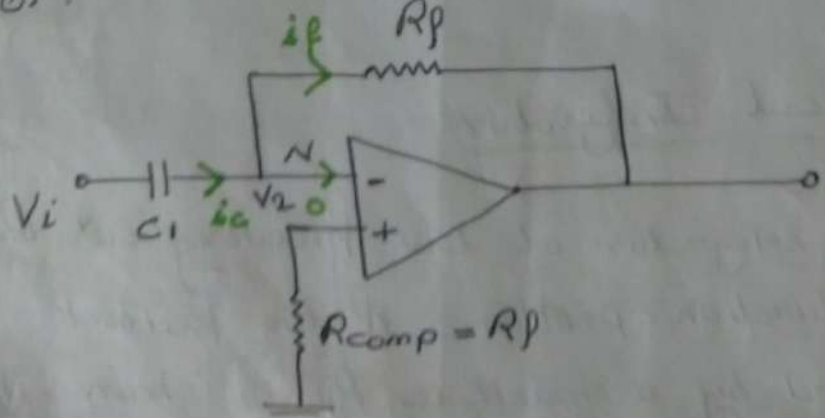
The gain of an integrator at low frequency can be limited to avoid the saturation problem if the feedback capacitor is shunted by a resistance Rf as shown. The parallel combination of Rf & Cf behaves like a practical capacitor which dissipates power unlike an ideal capacitor. For this reason, this ckt is also called a lossy integrator. This R_f limits the low frequency. Provides dc stabilization



Here R_f is connected parallel to 'C_f' ie, when V_i falls to zero, only dc offset voltage is present at o/p. DC voltage cannot pass through C_f $\therefore$ ckt becomes open loop. So its stability decreases, in order to overcome this, R_f is provided to have an alternate path. Thus there is an error voltage at o/p to reduce this error volt.

Differentiator

The ckt in which the o/p waveform is the derivative of the i/p waveform is the differentiator or differential amplifier.



$$V_o = -R_f C_1 \frac{dV_i}{dt}$$

$$\left\{ \begin{array}{l} i_c - i_f - 0 = 0 \\ i_c = i_f \end{array} \right.$$

Consider the node 'N' $\quad i_c = i_f$

$$i_c = C_1 \frac{d}{dt}(V_i - V_2)$$

$$i_f = \frac{V_o - V_2}{R_f}$$

$i_f = V$

Since V_2 is the virtual ground

$$\frac{C_1 dV_i}{dt} = \frac{-V_o}{R_f}$$

$$V_o = -R_f C_1 \frac{dV_i}{dt}$$

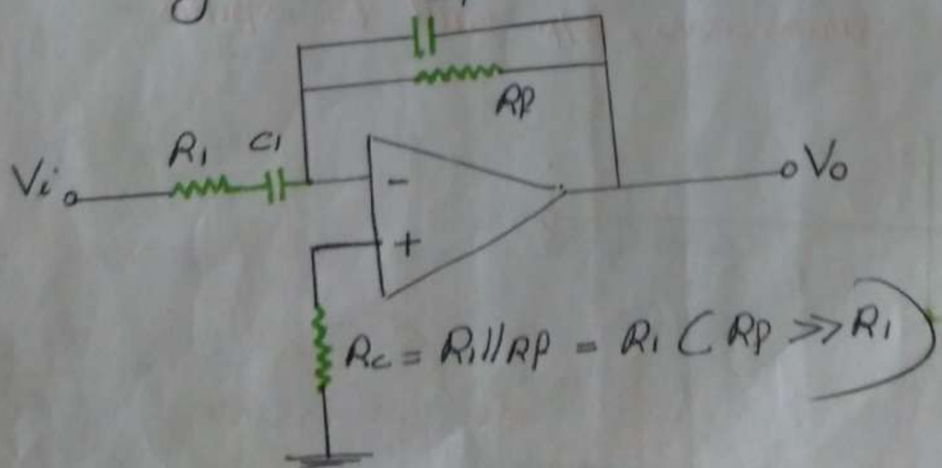
Thus the o/p voltage is $-R_f C_1$ times derivative of i/p voltage. The o/p is 180° out of phase with i/p.

⇒ At high frequency a differentiator may become unstable & break into oscillations.

⇒ Also the i/p impedance ($1/\omega C$) decreases with the increase in frequency thereby making the ckt sensitive to high frequency noise.

Practical Differentiator ckt

This ckt will eliminate the problem of stability & high frequency noise.



⇒ Here as gain increases it will lead to unstability so a capacitor 'Cf' is connected

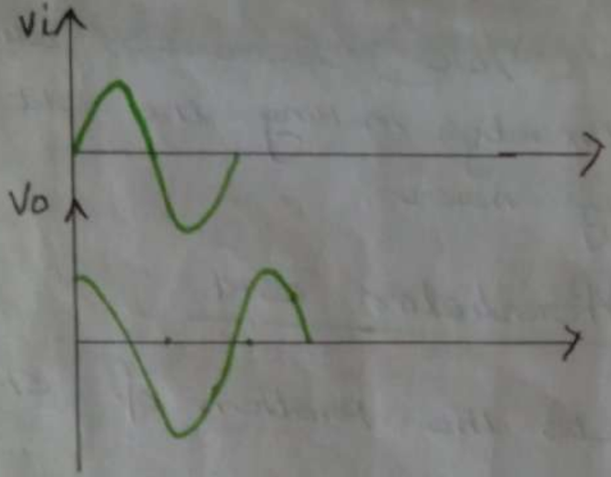
⇒ Inorder to avoid noise disturbance R_1 is connected

$$f_b = \frac{1}{2\pi R_1 C_1}$$

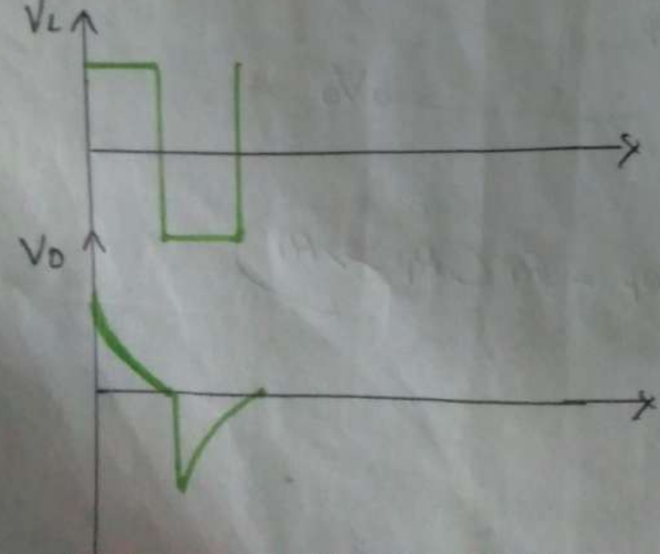
The change in gain is caused by R_1C_1 & R_fC_f.

⇒ Thus the gain at high frequency is reduced significantly there by avoiding the high frequency noise & stability problem.

* If the i/p sine wave, o/p will be cosine



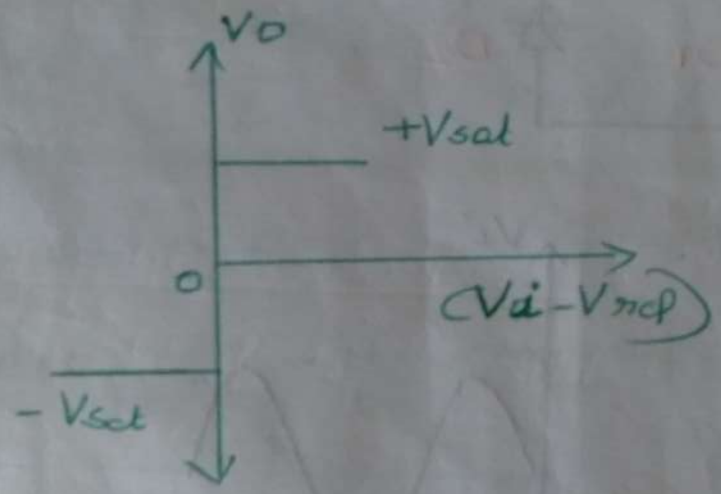
* If the i/p square wave, o/p will be spikes



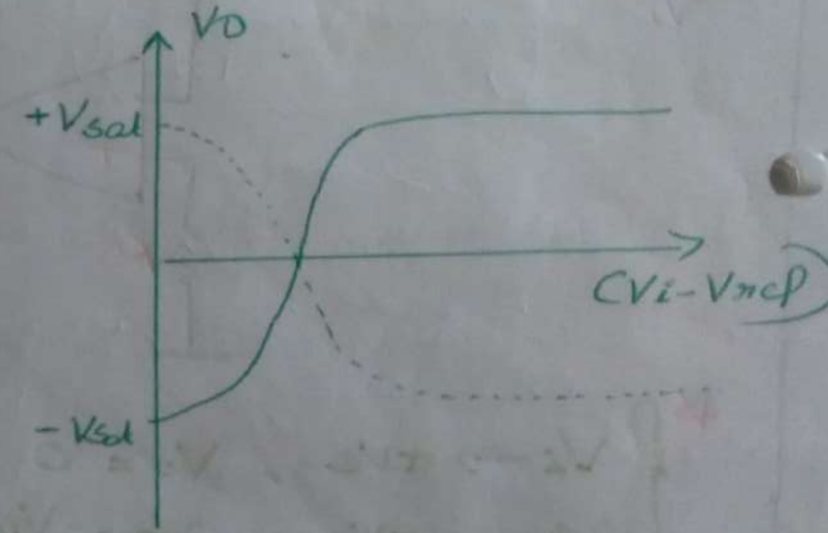
Comparator

A comparator is a ckt which compares a signal voltage applied at one i/p of an op-amp with a known reference voltage at other i/p

Ideal Comparator



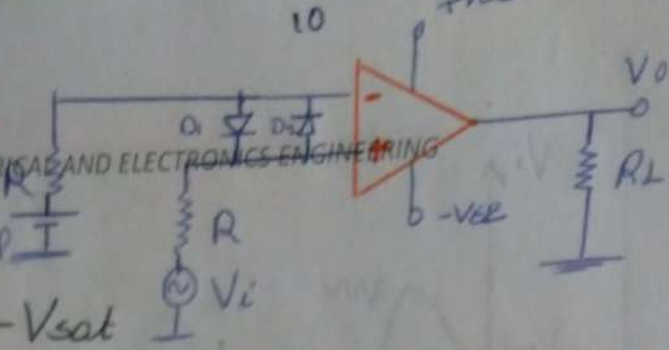
Practical Comparator



Two types of comparators

1) Non Inverting Comparator.

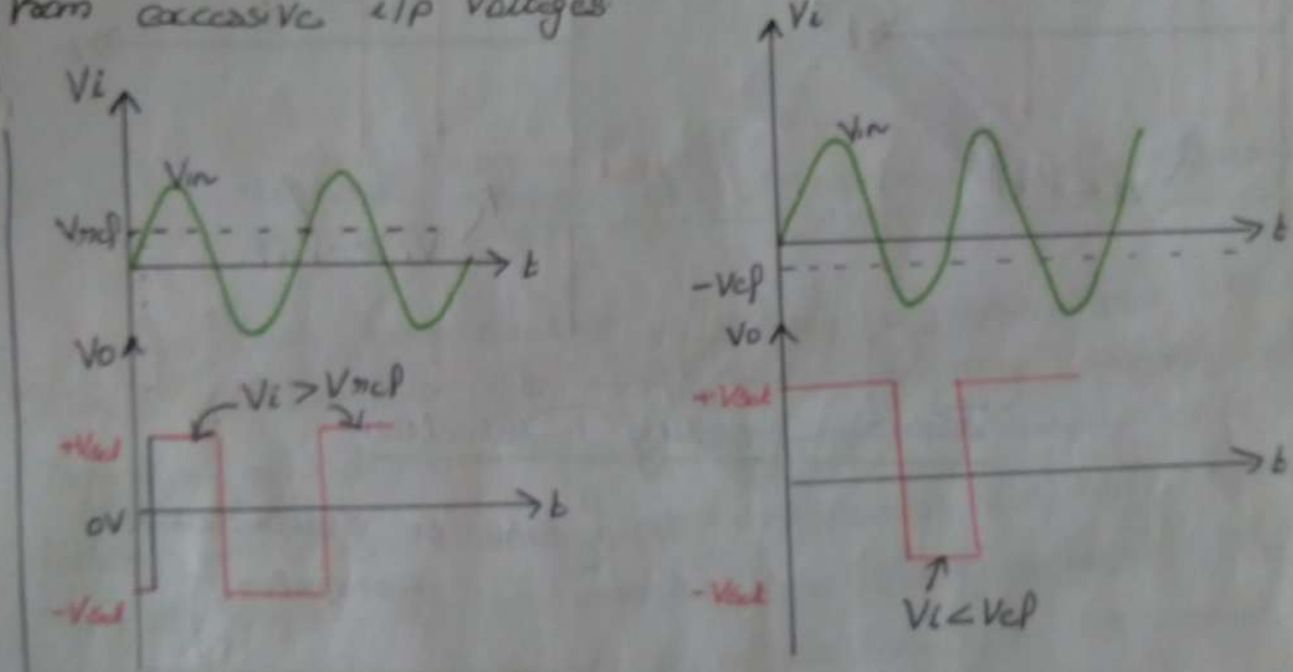
A fixed reference voltage V_{ref} is applied to the inverting i/p terminal & a time varying signal 'V_i' is applied to the non-inverting terminal.



When $V_i < V_{ref}$, then V_o is at $-V_{sat}$

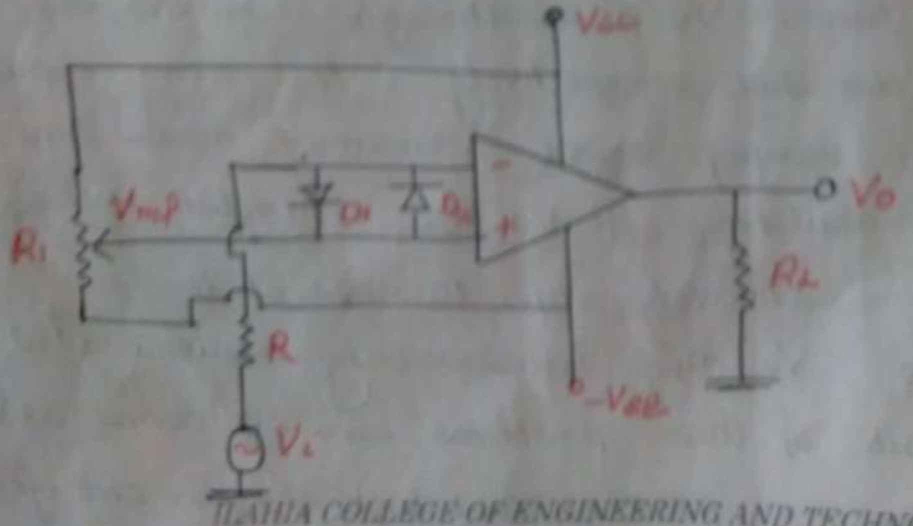
Either $V_i > V_{ref}$, then V_o is at $+V_{sat}$

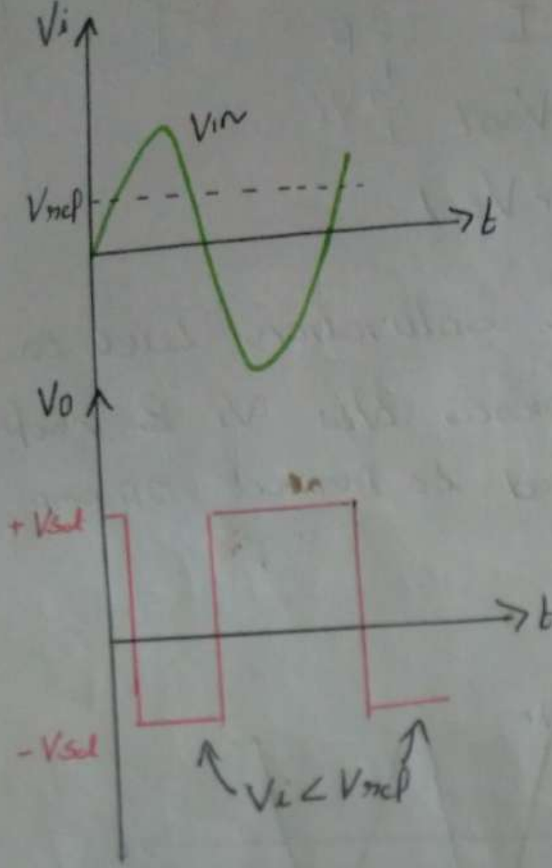
Thus o/p changes from one saturation level to another depending upon the difference b/w V_i & V_{ref}. The diodes D_1 & D_2 are connected to protect op-amp from excessive i/p voltages

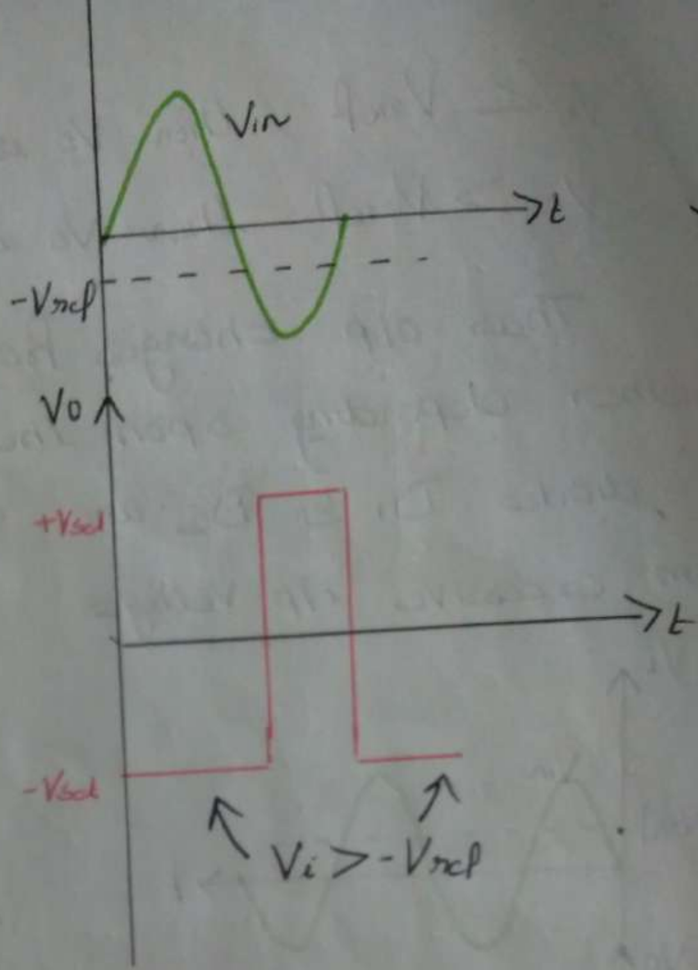


2) Inverting Comparator

Here V_{ref} is applied to (+) i/p & V_i is applied to (−) i/p



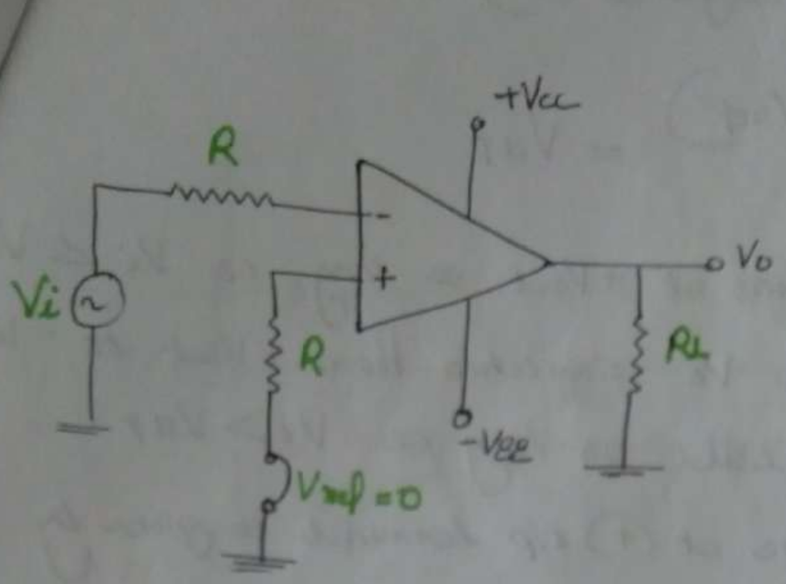


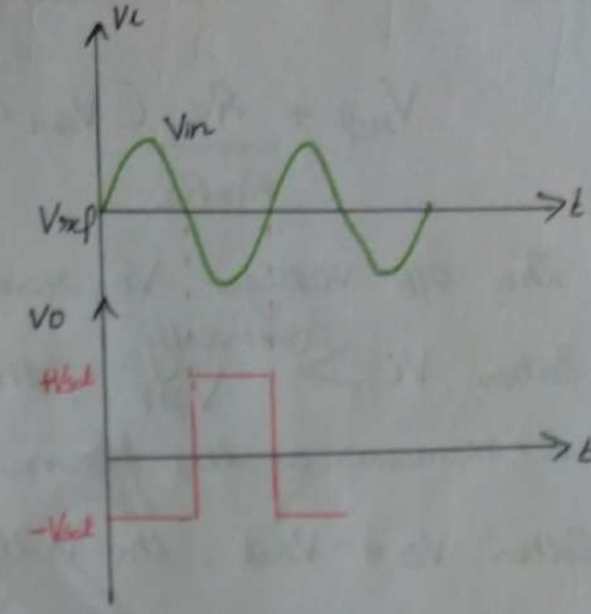


Zero Crossing Detector

{ Sine to square wave converter }

The V_{ref} is set to zero & i/p sine wave (V_i) is applied to (−) i/p terminal. The o/p wave form switches b/w +ve & −ve saturation levels, when V_i passes through zero in the negative & positive direction respectively. In some applications V_i may be a slow varying signal consuming more time to cross 0V. Thus switching of V_o b/w saturation voltages takes longer time. Conversely due to noise at the i/p terminal of op-amp, V_o may unnecessarily switches b/w $+V_{sat}$ & $-V_{sat}$. Both of these problems can overcome with the use of regenerative or positive feed back in the ckt of Schmitt Trigger.





Schmitt Trigger or Regenerative Comparator

The basic comparator is used in open loop mode. Since the openloop gain of op-amp is very large, false triggering at o/p can occur even due to small milli volts either i/p changes slowly as compared to o/p, noise is coupled from o/p of comparator back to i/p. The comparator ckt designed with positive f.b to avoid unwanted triggering is called Schmitt Trigger or Regenerative Comparator.

The i/p voltage is applied to (-) i/p terminal & f.b to (+) i/p terminal. The i/p voltage V_i triggers the o/p V_o everytime, it exceeds certain voltage levels. These voltages are called upper & lower threshold voltages $\{V_{UT}, V_{LT}\}$. The diff b/w V_{UT} & V_{LT} is called hysterisis voltage

$$V_H = V_{UT} - V_{LT}$$

Suppose $V_0 = +V_{sat}$, then voltage at (+) i/p terminal is

$$V_{ref} + \frac{R_2}{R_1+R_2}(V_{sat} - V_{ref}) = V_{UT}$$

The o/p voltage V_0 remains at $+V_{sat}$ as long as $V_i < V_{UT}$.

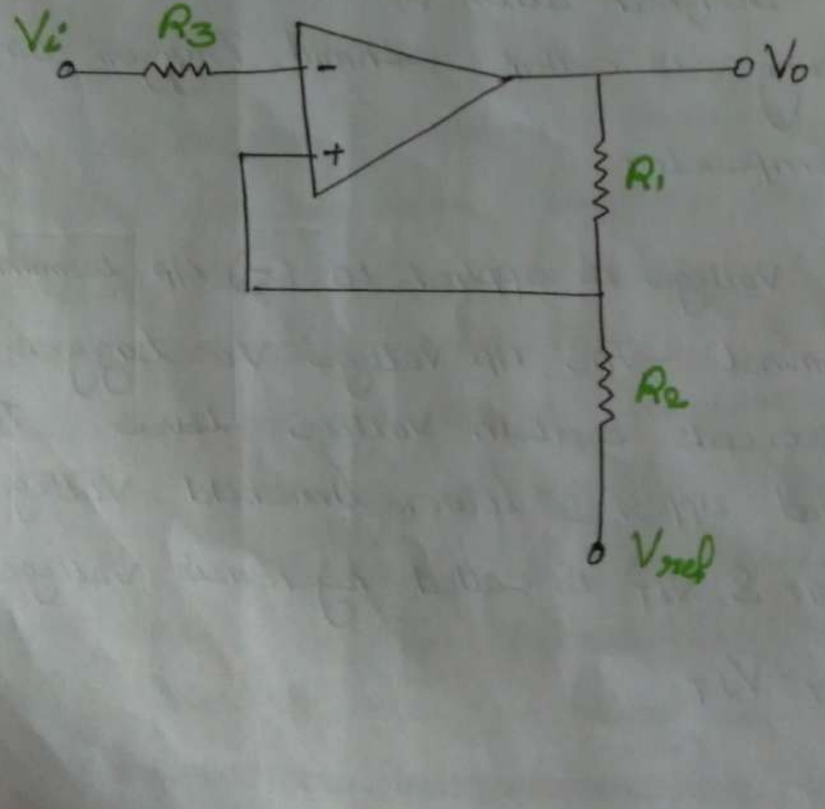
When $V_i \overset{\text{significantly}}{>} V_{UT}$, then V_0 switches from $+V_{sat}$ to $-V_{sat}$ & remains at the same level as long as $V_i > V_{UT}$.

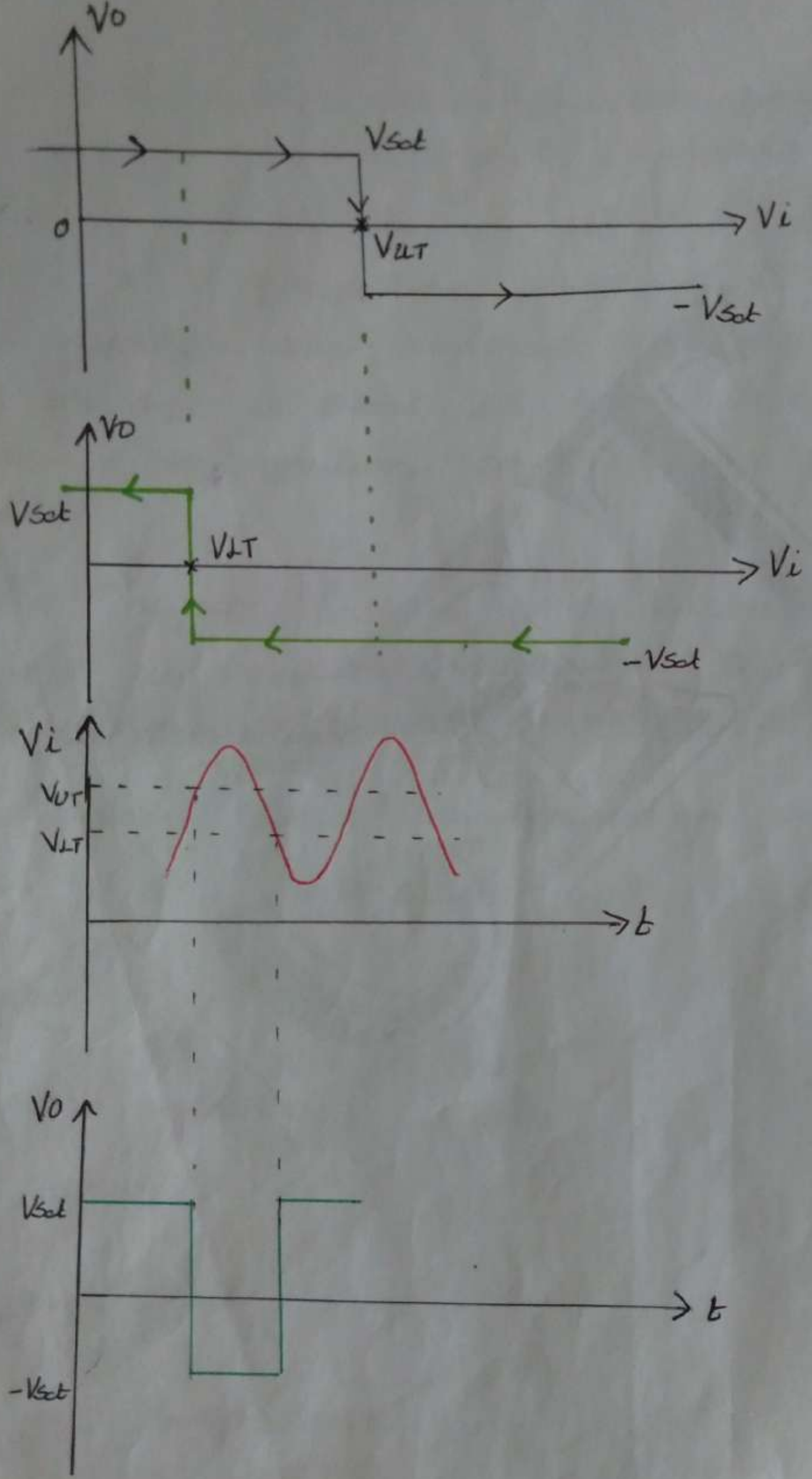
When $V_0 = -V_{sat}$, the voltage at (+) i/p terminal is given by

$$V_{ref} - \frac{R_2}{R_1+R_2}(V_{sat} + V_{ref}) = V_{LT}$$

When $V_i \overset{\text{slightly}}{<} V_{LT}$, V_0 switches from $-V_{sat}$ to $+V_{sat}$

Hysteresis width $V_H = V_{UT} - V_{LT} = \dfrac{2R_2 V_{sat}}{R_1+R_2}$

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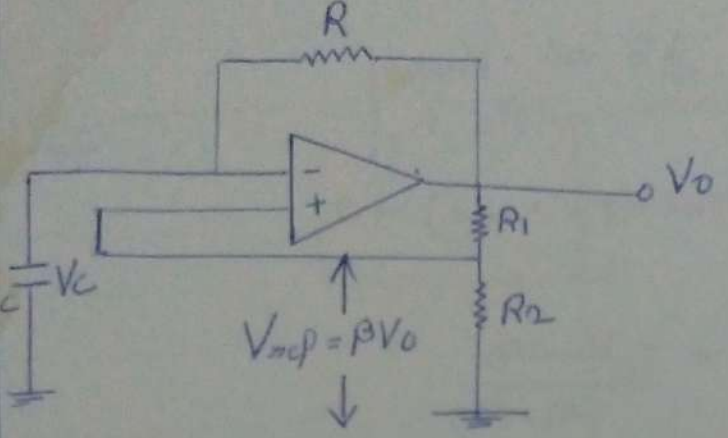
Square Wave Generator or Astable Multivibrator Using Op-



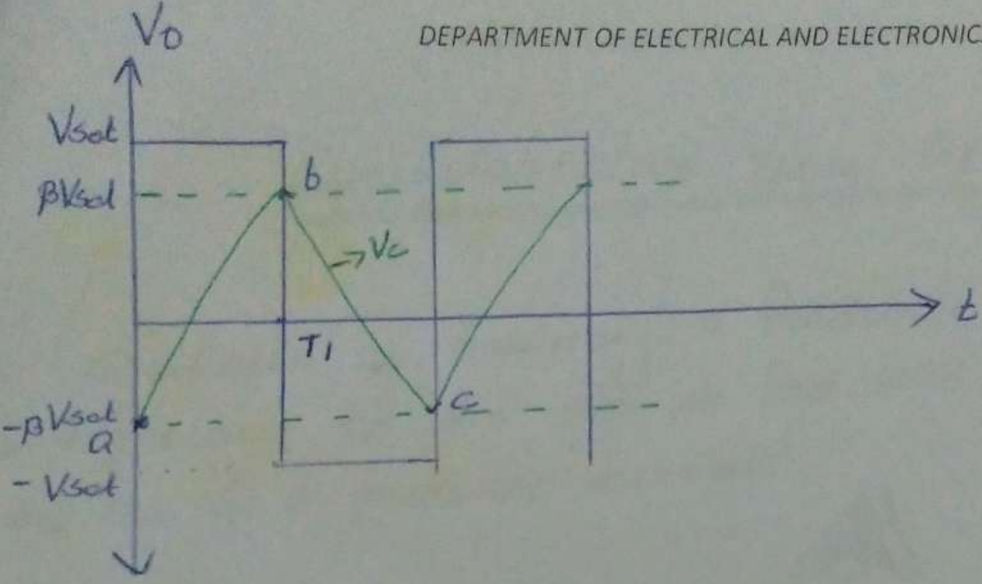
The fig shows astable multivibrator with o/p of op-amp feedback to (+) i/p terminal. The resistors R_1 & R_2 form a voltage divider n/w & a fraction $\beta = \frac{R_2}{R_1+R_2}$ of o/p is feedback to i/p.

Let o/p is at $+V_{sat}$

⇒ then 'C' charges through R towards $+V_{sat}$. The voltage at '+' i/p terminal is at $+\beta V_{sat}$. The charging of 'C' continues until V_c is just greater than voltage at (+) i/p terminal. When this happens at pt 'b' the o/p switched down to $-V_{sat}$

o/p is now at $-V_{sat}$

⇒ Then the capacitor 'C' starts discharging towards $-V_{sat}$. At pt 'c' V_c just exceeds $-\beta V_{sat}$, then o/p switches back to $+V_{sat}$



The voltage across capacitor

$$V_c(t) = V_{fin} + (V_{ini} - V_{fin})\, e^{-t/RC}$$

$$= V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

At $t = T_1$,

$$\beta V_{sat} = V_{sat}\left(1 - (1+\beta)\, e^{-T_1/RC}\right)$$

$$(1-\beta) = (1+\beta)\, e^{\frac{-T_1}{RC}}$$

$$\Rightarrow T_1 = RC \ln \frac{1+\beta}{1-\beta} = RC \ln \frac{R_1 + 2R_2}{R_1}$$

Total time period, $T = 2T_1 = \underline{2RC \ln \frac{R_1 + 2R_2}{R_1}}$

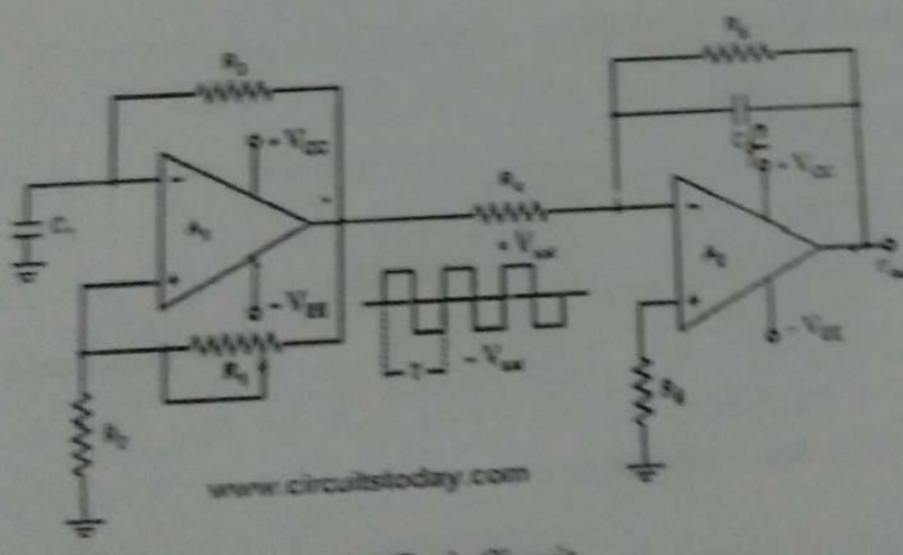
$$f = 1/T = \frac{1}{2RC \ln \frac{R_1 + 2R_2}{R_1}}$$

RAMP GENERATOR

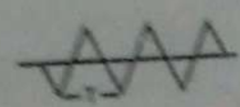
If the step input of the integrating amplifier is replaced by a continuous time square wave, the change in the input signal amplitude charges and discharges the feedback capacitor. This results in a triangular wave output with a frequency that is dependent on the value of (R_i.C_f), which is referred to as the time constant of the circuit. Such a circuit is commonly called a Ramp Generator.

During the positive half-cycle of the square wave input, a constant current I flows through the input resistor Rf. Since the current flowing into the op-amp internal circuitry is zero, effectively all of the current flows through the feedback capacitor C_f. This current charges the capacitor. Since the capacitor connected to the virtual ground, the voltage across the capacitor is the output voltage of the op-amp.

During the negative half-cycle of the square wave input, the current I is reversed. The capacitor is now linearly charged and produces a positive-going ramp output.



(a) Basic Circuit



(b) Output Waveform

Triangular Wave Generator

The triangular wave generator consists of two op-amp & several passive components. A_1 is a Schmitt Trigger ckt which generate a square pulse. A_2 is an integrator which integrates the o/p of Schmitt Trigger to produce a triangular wave.

Let us consider the o/p V_o' of A_1 is at $+V_{sat}$ initially & produces a negative going ramp at o/p (V_o). Hence the voltages at two ends of voltage divider formed by $R_2 - R_1$ are V_{sat} & V_{ramp}. At $t = T_1$, when a negative going ramp reaches $-V_{ramp}$ at Pt 'a', the voltage at Pt 'P' becomes slightly less than 0V. This switches A_1 to its negative saturation level $-V_{sat}$. With the o/p of A_1 at $-V_{sat}$, A_2 starts integrating & increases the o/p in positive direction. At $t = T_2$ at Pt 'b' the voltage at Pt 'P' becomes greater than 0V & switches V_o' to $+V_{sat}$. This cycle repeats.

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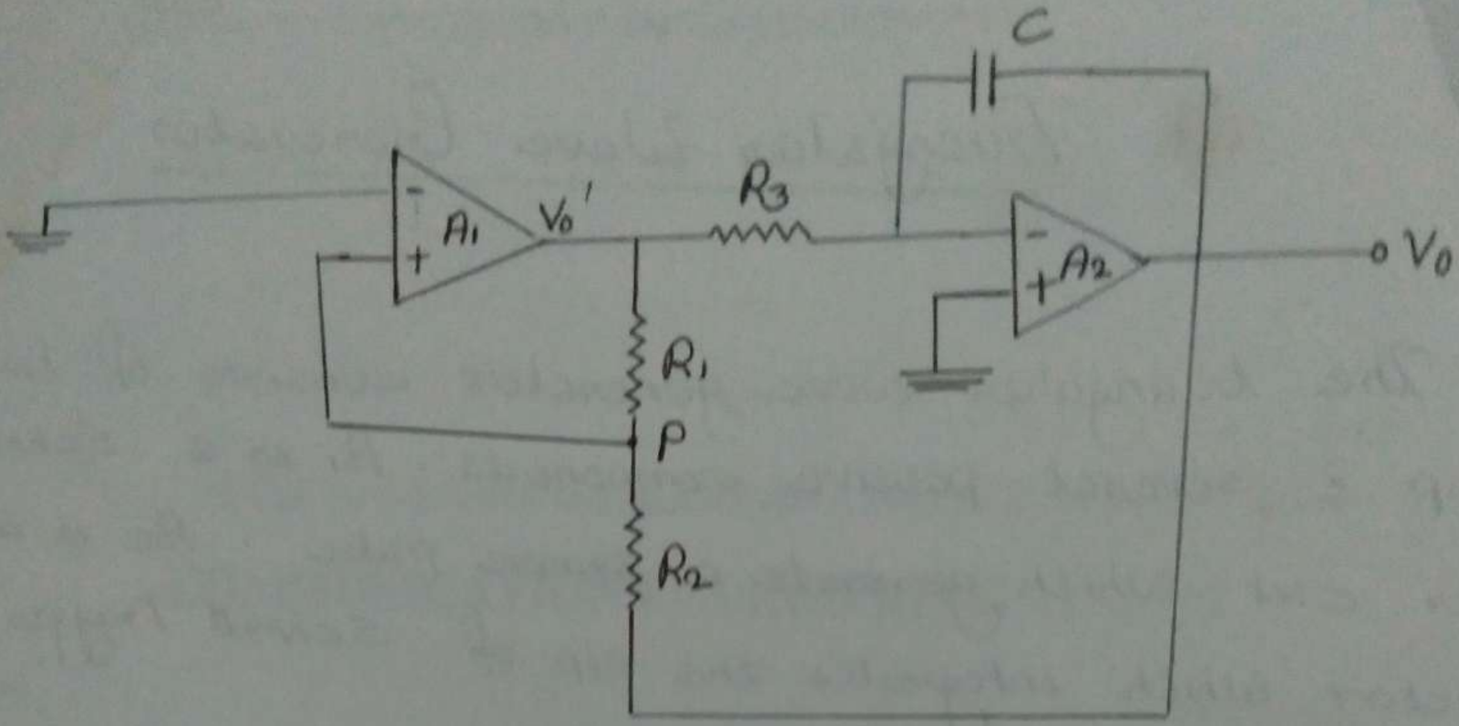
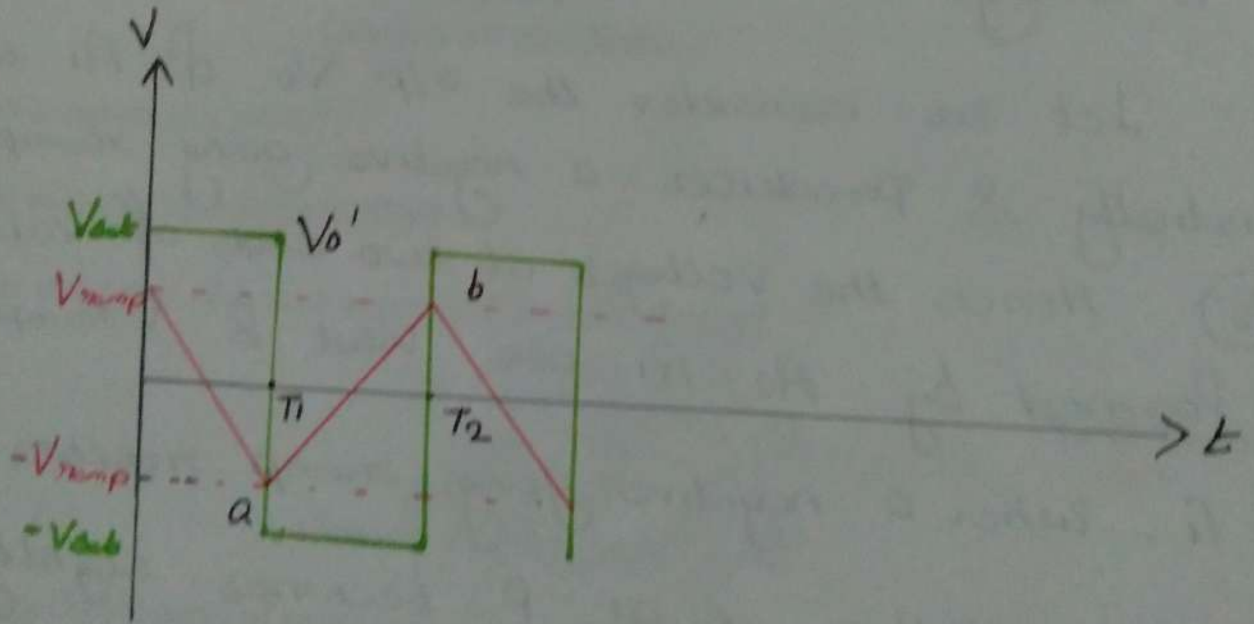
$$\boxed{T = \frac{4R_2R_3C}{R_1} \qquad f = \frac{1}{T} = \frac{R_1}{4R_2R_3C}}$$





Explain

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