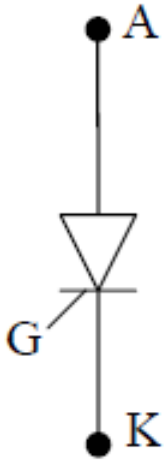
Module I

- SCR-Structure, static characteristics & switching (turn-on & turn-off) characteristics
- - di/dt & dv/dt protection –
- turnon methods of SCR - two transistor analogy - series and parallel connection of SCRs -Structure and principle of operation of power diode, TRIAC,GTO, Power MOSFET & IGBT – Comparison

SCR (Silicon Controlled Rectifier)

- Four layer, three junction, p-n-p-n semiconductor switching device.
- Basically a thyristor consist of 4 layers of alternate p-type and n-type silicon semiconductors forming three junctions J1, J2 and J3



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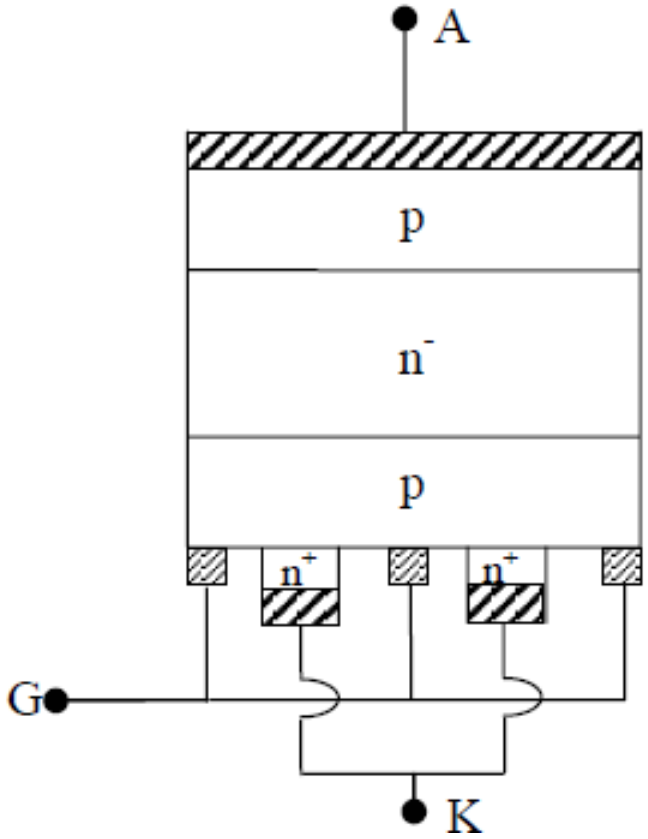
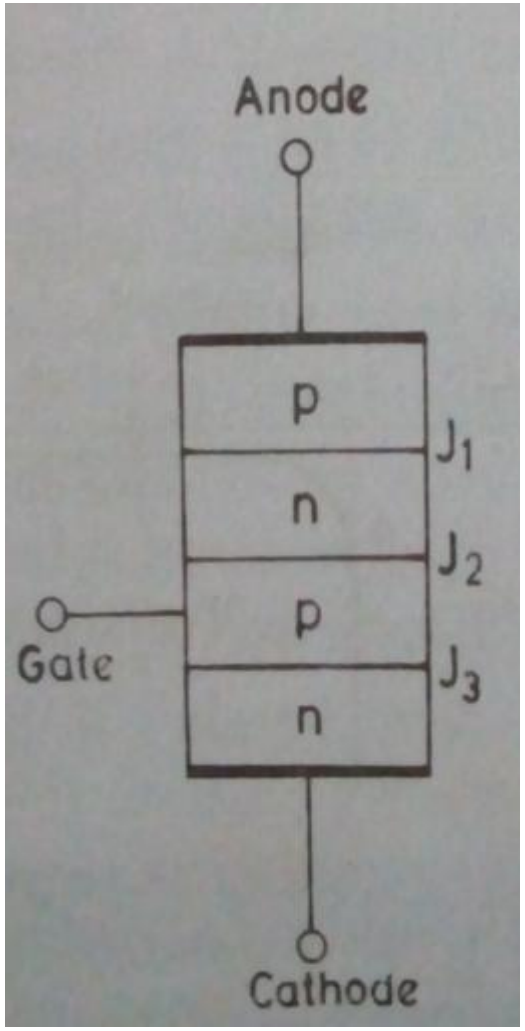




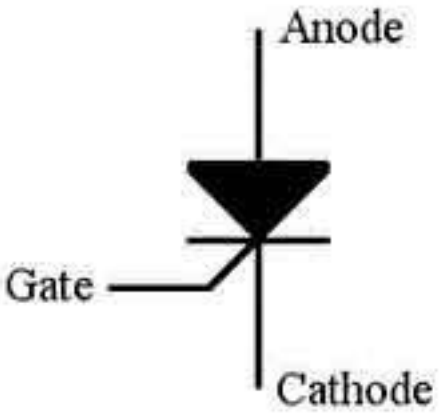
SCR (Silicon Controlled Rectifier)

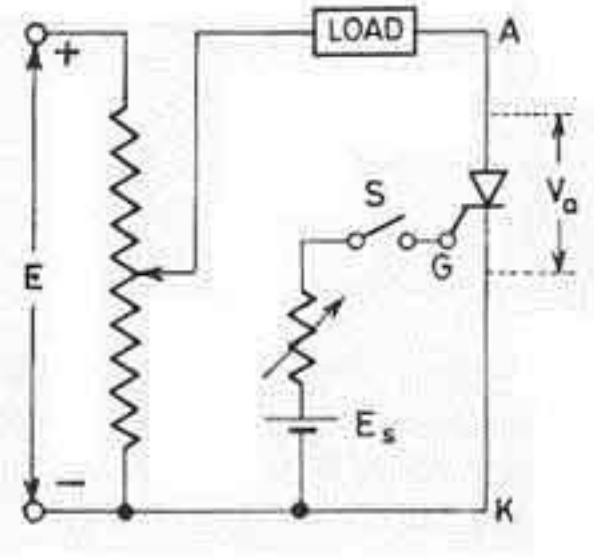
- Gate terminal is usually kept near the cathode terminal
- The terminal connected to outer p region is called the anode
- The terminal connected to outer n region is called the cathode and that connected to inner p region is called gate
- For large current applications thyristors need better cooling, this is achieved to great extent by mounting them onto heat sinks
- SCRs of voltage rating 10kV and an r.m.s current rating of 3000A with corresponding power handling capacity of 30MW are now available
- Such a high power thyristor can be switched on by a low voltage supply of about 1A and 10W

- An SCR is so called because silicon is used for its construction and its operation as a rectifier can be controlled
- Like the diode SCR is a unidirectional device, that blocks the current flow from cathode to anode
- Unlike the diode, a thyristor also blocks the current flow from anode to cathode until it is triggered into conduction by a proper gate signal between gate and cathode terminal

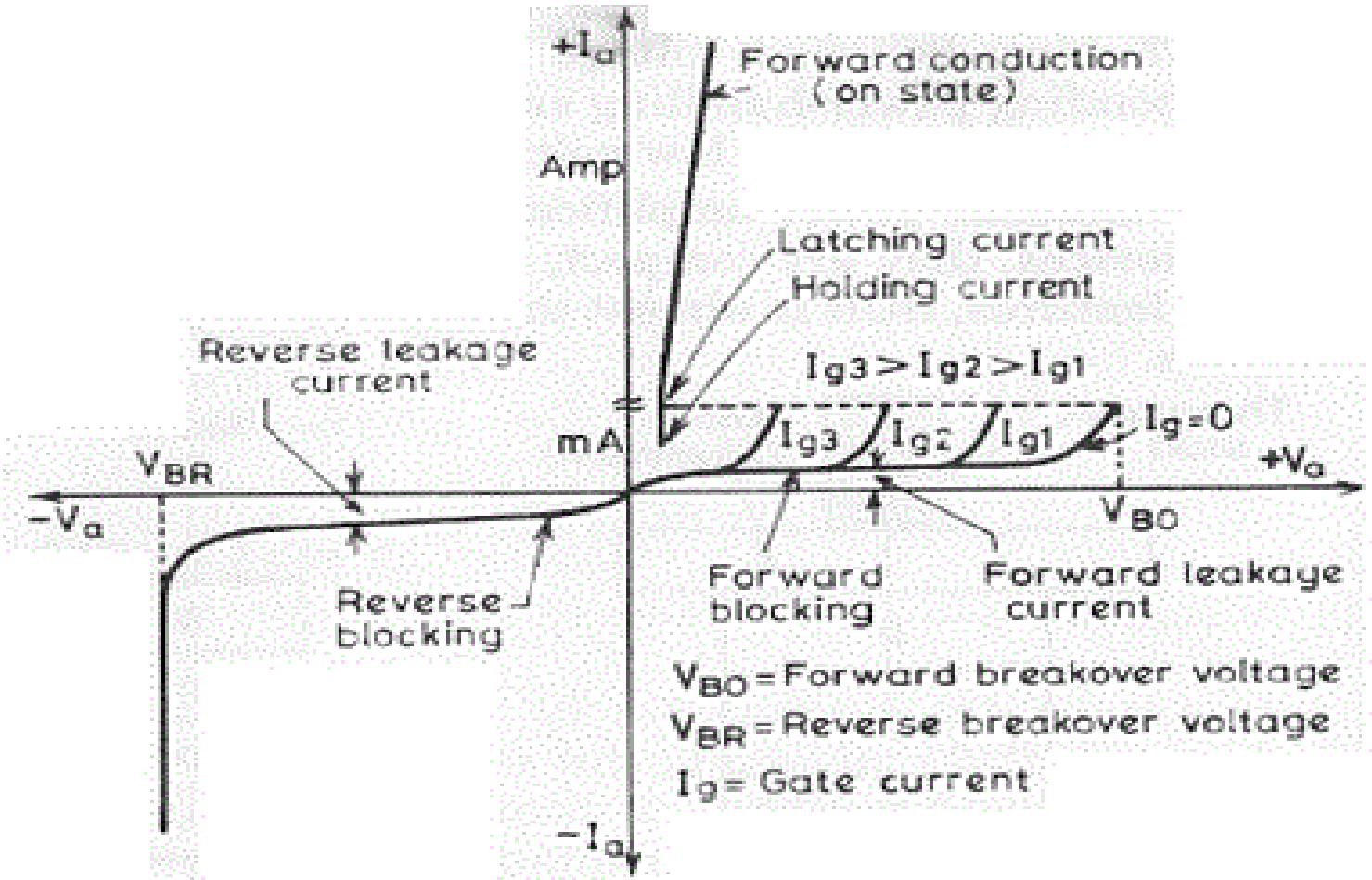
SCR – Static V-I Characteristics

- An elementary circuit diagram for obtaining static V-I characteristics of a thyristor is shown below
- The anode and cathode are connected to main source through load
- The gate and cathode are fed from a source of Es which provides +ve gate current from gate to cathode





Thyristor Symbol Circuit diagram of thyristor.



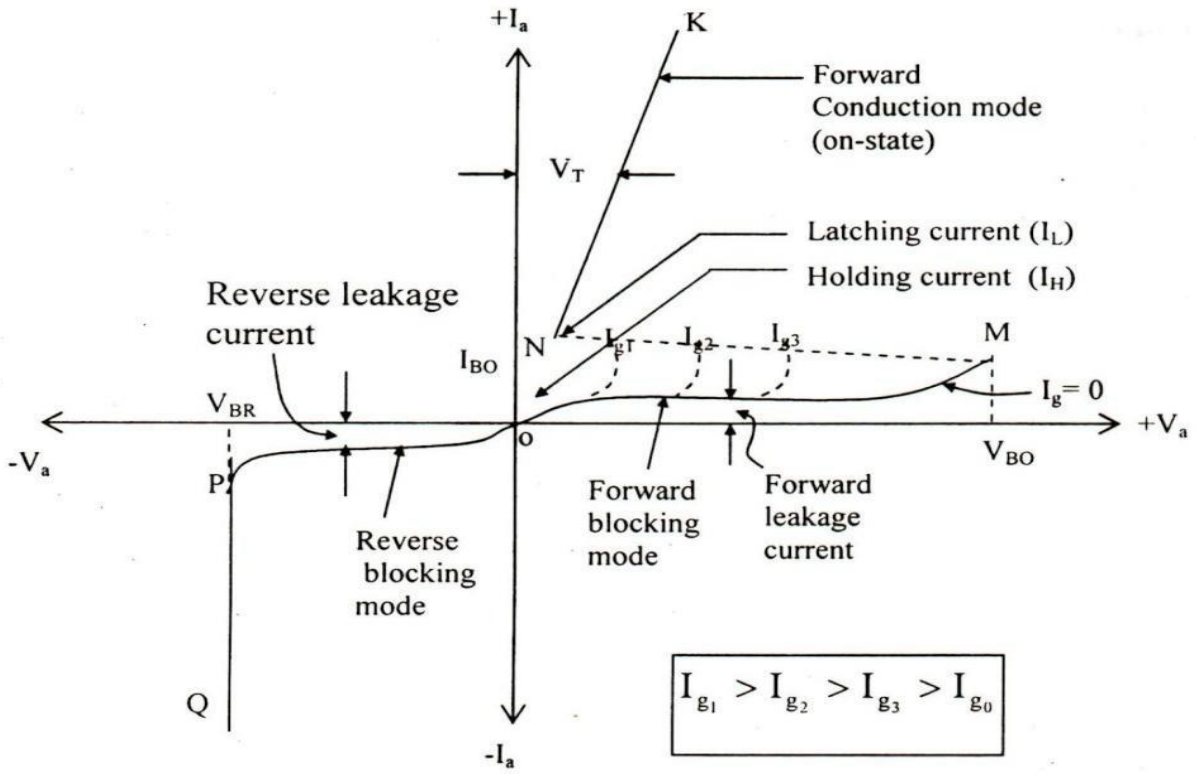
V-I characteristics of thyristor.

The characteristics reveals that a thyristor has three basic modes of operation

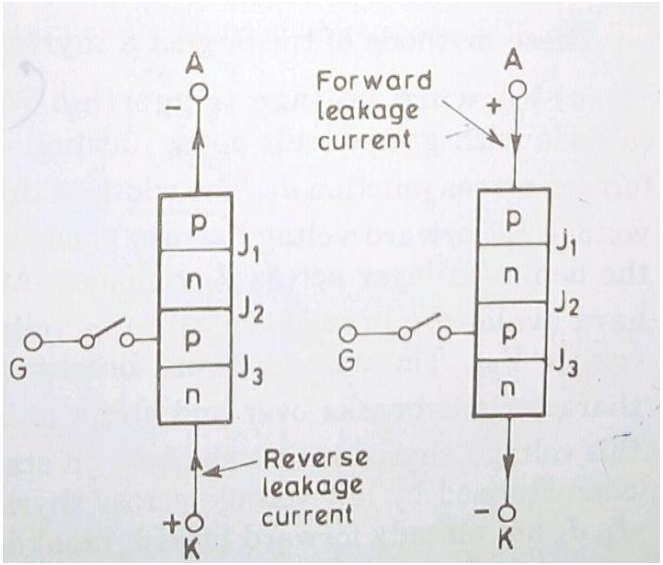
Reverse blocking mode

Forward blocking mode (off state)

Forward conduction mode (on state)



- Reverse blocking mode
- When cathode is made +ve w.r.t anode with switch S open thyristor is reverse biased Junction
- J1 and J3 are seen to be reverse biased
- A small leakage current of the order of a few milli-amperes flows. This is reverse blocking mode, called the off state of a thyristor
- If the reverse voltage is increased, then at a critical breakdown
- level, called reverse breakdown voltage VBR, an avalanche occur at J1 and J3
- Reverse current increases rapidly



Forward blocking mode

- When anode is +ve w.r.t cathode, with gate circuit open,thyristor is said to be forward biased
- J1 and J3 are forward biased
- J2 is reverse biased
- In this mode, a small current called forward leakage current flows
- As the forward leakage current is small, SCR offer a high impedance
- Therefore a thyristor can be treated as an open switch even in the forward blocking mode

Forward conduction mode

- When anode to cathode forward voltage is increased with gate circuit open, reverse biased junction J2 will have an avalanche breakdown at a voltage called forward break-over voltage VBO
- After this breakdown thyristor gets turned on with point M at once shifting to N and then to a point where between N and K
- Here NK represents the forward conduction mode
- A thyristor can be brought from forward blocking mode to forward conduction mode by turning on by applying

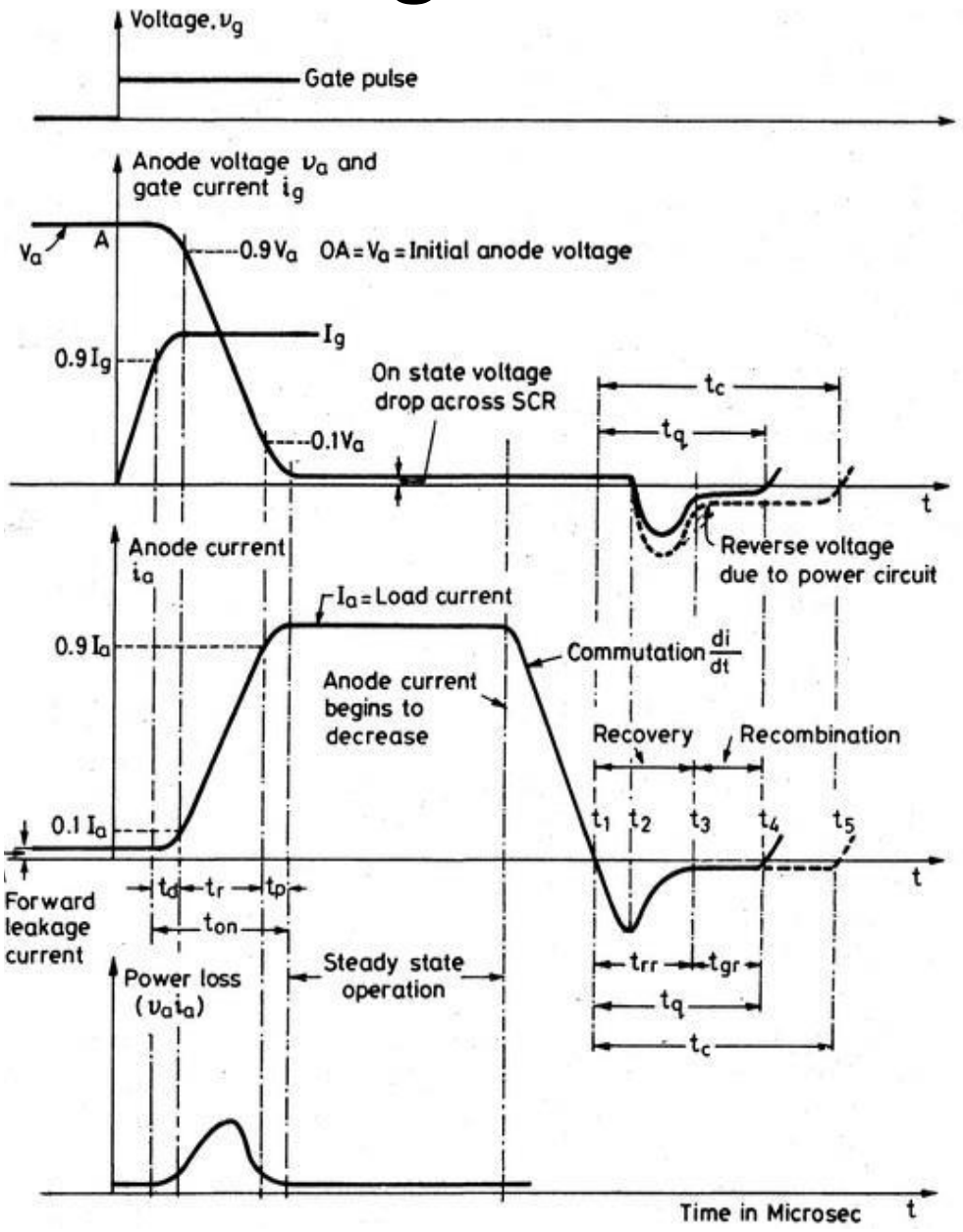
  1)A positive gate pulse between gate and cathode

  2)A forward break-over voltage across anode and cathode

SCR – Switching Characteristics

- During turn on and turn off process a thyrisor is subjected to different voltages across it and different currents through it
- The time variation of a voltage across a thyristor and the current through it during turn on and turn off process gives the dynamic or switching characteristics of a thyristor

SCR – Switching Characteristics



Switching characteristics during turn on

- A forward biased thyristor is usually turned on by applying a +ve gate voltage between gate and cathode . There is however a transition time form forward off state to forward on state.
- This transition time is called thyristor turn on time Is defined as the time during which it changes from forward blocking state to final on state
- The turn on time can be divide into three intervals
- Delay time td
- Rise time tr
- Spread time tp

Delay time td

- Measured from the instant at which gate current reaches 0.9Ig to the instant at which anode current reaches 0.1Ia
- Ig and Ia are the final values of gate and anode currents
- It can also be defined as the time during which anode voltage falls from Va to 0.9Va.Va is the initial value of anode voltage
- Another way of defining is the time during which anode Current rises from forward leakage current to 0.1Ia, where Ia is the final value of anode current

- With the thyristor initially in the forward blocking state the anode voltage is OA and anode current is small leakage current
- Initiation of turn on process is indicated by a rise in anode current from small leakage current and a fall in anode cathode voltage from forward blocking voltage OA
- As gate current begins to flow from gate to cathode with the application of gate signal, the gate current has non-uniform distribution of current density over cathode surface due to the p layer
- During delay time anode current flows in a narrow region near the gate where gate current density is the highest
- The delay time can be reduced by applying high gate current and more forward voltage between anode and cathode
- The delay time is fraction of microsecond

Rise time

- Is the time taken by the anode current to rise form 0.1Ia to 0.9Ia
- Time required for the forward blocking off state voltage to fall from 0.9 to 0.1 of its initial value
- Rise time is inversely proportional to the magnitude of gate current and its build up rate
- Rise time can be reduced if high and steep current pulses are applied to the gate
- The main factor determining the tr is the nature of anode circuit

- During rise time turn on losses in the thyristor are the highest due to high anode voltage and large anode current occurring together in the thyristor
- As these losses occur only over a small conducting region,local hot spot may be formed
- And the device may be damaged

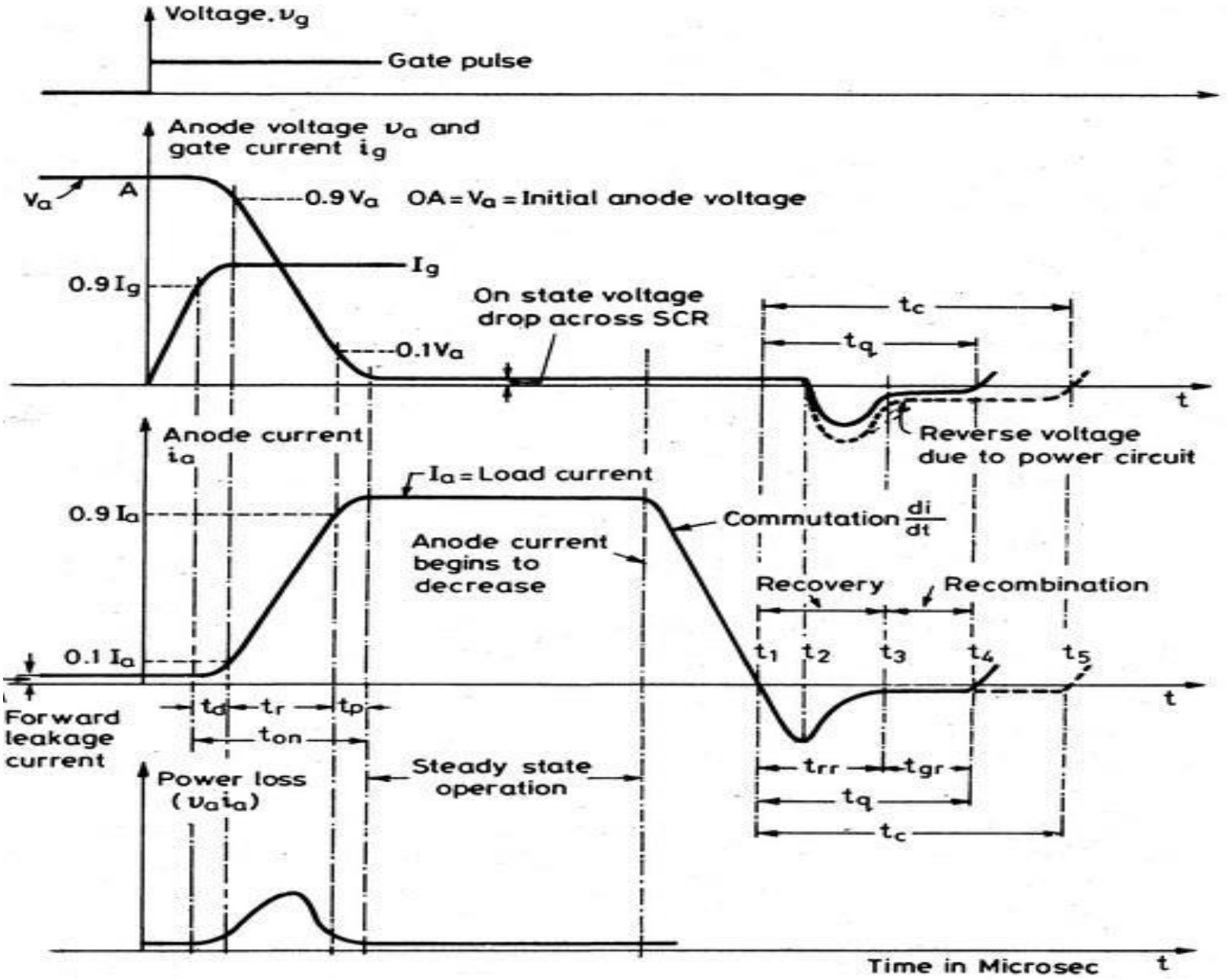
Spread time

- Time taken by the anode current to rise from 0.9Ia to Ia
  Time for the forward blocking voltage to fall from 0.1 of its initial value of its on state voltage drop (1 to 1.5V)
- During this time conduction spreads over entire cross section of the cathode of SCR
- After the spread time anode current attains steady state value and the voltage drop across SCR is equal to the on state voltage drop of the order of 1 to 1.5V
- Total turn on time of an SCR is equal to the sum of delay time, rise time and spread time
- Manufactures usually specify the rise time which is of the order of 1 to 4µ sec
- Total turn on time depends on the anode circuit parameters and gate signal wave-shapes

Switching characteristics duringTurn off

- Turn off means that it has changed from on to off state and is capable of blocking the forward voltage
- This dynamic process of SCR from conduction state to forward blocking state is called commutation process or turn off process
- Once the thyristor is on, gate loses control the SCR can be turned off by reducing the anode current below holding current
- The turn of time tq of a thyristor is defined as the time between the instant anode current become zero and the instant SCR regains forward blocking capability

- During time tq, all the excess carriers from the four layers of SCR must be removed.
- This removal of excess carriers consisting of sweeping out of holes from outer p layer and electrons from outer n layer
- The carriers around junction J2 can be removed only by
- recombination
- The turn off time is divided into two interval
- 1) Reverse recovery time trr
- 2) Gate recovery time tgr
- tq=trr+tgr


Voltage, v_g
Gate pulse
Anode voltage v_a and gate current i_g
V_a
A
0.9 V_a
OA = V_a = Initial anode voltage
I_g
0.9 I_g
On state voltage drop across SCR
0.1 V_a
t_c
t_q
t
Reverse voltage due to power circuit
Anode current i_a
I_a = Load current
0.9 I_a
Commutation $\frac{di}{dt}$
Anode current begins to decrease
Recovery
Recombination
t_1 t_2 t_3 t_4 t_5
0.1 I_a
Forward leakage current
t_d t_r t_p
t_{on}
Power loss ($v_a i_a$)
Steady state operation
t_{rr} t_{gr}
t_q
t_c
Time in Microsec
t

Reverse recovery time

- At instant t1, anode current becomes zero
- After t1, anode current build up in the reverse direction
- The reason for the reversal of anode current after t1 is due to the presence of carriers stored in the four layers
- The reverse recovery current removes excess carriers from the end junction J1 and J3 between the instant t1 and t3
- In other words, reverse recovery current flows due to the
- sweeping out of holes from top p layer and electrons from bottom layer
- At instant t2, when about 60% of the stored charges are removed from the outer two layers carrier density across J1 and J3 begins to ecrease and with this reverse recovery current also starts decaying

- The reverse current decay is fast in the beginning but gradual thereafter
- The fast decay of the recovery current causes a reverse voltage across the device due to the circuit inductance
- This reverse voltage surge may cause damage to the device
- In practice this avoided by using protective RC element across SCR
- At instant t3, when reverse recovery current has fallen nearly to zero, end junction J1 and J3 recover and SCR is able to block the reverse voltage

Gate recovery time

- At the end of reverse recovery period (t1-t3), the middle junction J2 still has trapped charges therefore, the thyristor is not able to block the forward voltage at t3
- The trapped charges around J2 cannot flow to the external circuit
- Therefore this charges must decay only by recombination
- This recombination is possible if a reverse voltage is maintained across SCR The rate of recombination of charges is independent of the external circuit parameter
- The time for recombination of charges between t3 and t4 is called gate recovery time tgr

- At instant t4, junction J2 recovers and the forward voltage can be reapplied between anode and cathode
- The turn off time provided to a thyristor by the practical

  circuit is called circuit turn off time tc
- Is defined as the time between the instant anode current

  become zero and the instant reverse voltage due

  to practical circuit reaches zero
- tc must be greater than tq for reliable turn off
- Otherwise the device may turn on at undesired instant, process called commutation failure

Thyristor protection

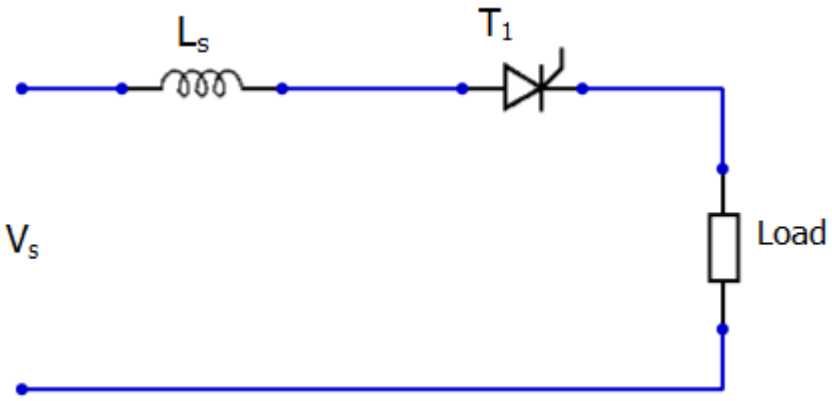
- Reliable operation of a thyristor demands that its specified ratings are not exceeded.In practice, a thyristor may be subjected to overvoltage or over-currents
- During SCR turn on, di/dt may be prohibitively large
- There may be false triggering of SCR by high value of dv/dt
- A thyristor must be protected against all such abnormal conditions for satisfactory and reliable operation of SCR circuit and the equipment

- **di/dt protection**
- When a thyristor is forward biased and is turned on by a gate pulse, conduction of anode current begins in the immediate neighborhood of the gate cathode junction
- Thereafter the current spread across the whole area of the junction
- The thyristor design permit the spread of conduction to the whole junction area as rapidly as possible
- However if the rate of rise of anode current i.e., di/dt is large as compared to the spread velocity of carriers, local hot spot will be formed near the gate junction.This localized heating may destroy the thyristor.
- Therefore the rate of rise of anode current at the time of turn on must be kept below the specified limiting value

- The value of di/dt can be maintained below acceptable limit by using a small inductor called, di/dt inductor in series with the anode circuit
- Typical di/dt limit values of SCR are 20 – 500 A/ μ sec
- Local hot spot heating can also be avoided by ensuring that the conduction spreads to the whole area as early as possible
- This can be achieved by applying agate current nearer to the maximum specified gate current

di/dt=Vs/Ls

Ls – series inductance including stray inductance



dv/dt protection

- If rate of rise of suddenly applied voltage across thyristor is high, the device may get turned on
- Such phenomena of turning on a thyristor is called dv/dt turn on And this must be avoided as it leads to false operation of the thyristor circuit
- For controllable operation of the thyristor, the rate of rise of anode to cathode voltage dVa/dt must be kept below the specified limit
- Typical value of dv/dt are 20 – 500V / μ sec
- False turn on of a thyristor by large dv/dt can be prevented by using a snubber circuit in parallel with the device

- *Snubber circuit*
- Consist of a series combination of resistance Rs and capacitance Cs in parallel with the thyristor
- Cs in parallel with the device is sufficient to prevent unwanted
- dv/dt triggering of the SCR
- When switch S is closed, a sudden voltage appear across the circuit Capacitor Cs behaves like a short circuit, therefore voltage across SCR is zero
- With the passage of time voltage across Cs builds up at a slow rate such that dv/dt across Cs and therefore across SCR is less than the specified maximum dv/dt rating of the device

- When the SCR is turned on capacitor discharges through the SCR and sends a current equal to Vs/ (resistance of the path formed by Cs and SCR)
- As this resistance is quite low, the turn di/dt will tend to be excessive and as a result SCR may be destroyed
- In order to limit the magnitude of discharge current a resistance Rs is inserted in series with Cs
- The value of snubber circuit constant τ=RsCs can be determined from for a known value of dv/dt.

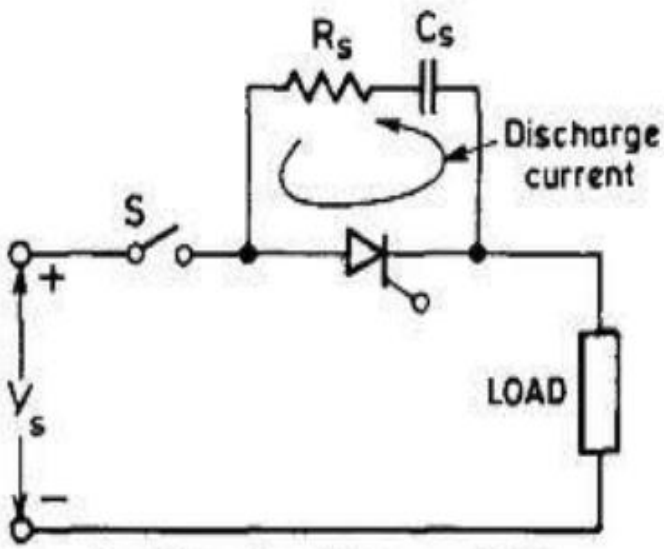
$$\frac{dv}{dt} = \frac{V_s}{R_s C_s}$$

- The value of Rs is found from

$$R_s = \frac{V_s}{I_{TD}}$$

- The discharging current

$$I_{TD} = \frac{V_s}{R_1 + R_2}$$



Snubber circuit across SCR.

Turn on methods of SCR

- With anode +ve w.r.t cathode, a thyristor can be turned on by any one of the following techniques

  Forward voltage triggering

  Gate triggering

  dv/dt triggering

  Temperature triggering

  Light triggering

Forward voltage triggering

- When forward voltage applied between anode and cathode with gate circuit open, junction J2 is reverse biased
- As a result depletion layer formed across J2
- The width of this layer decreases with an increase in anode - cathode voltage
- If forward voltage across anode-cathode is gradually increased, a stage come when depletion layer across j2 vanishes
- At this moment reverse biased junction J2 is said to have avalanche breakdown and the voltage at which this occur is called forward break-over voltage

- The name forward break-over voltage is given because at this voltage V_{BO} v-i characteristics break-over and shift to its on state position with brek-over current I_{BO}
- At this voltage, thyristor changes from off state (high voltage with low leakage current) to on state characterized by low voltage across thyristor with large forward current
- As other junction J1, J3 are already forward biased, breakdown of junction J2 allows free movement of carriers across three junctions and as a result large forward anode current flows
- This forward current is limited by load impedance
- In practice the transition from off state to on state obtained by exceeding V_{BO} is never employed as it may destroy the device

Gate triggering

- Turning on thyristor by gate triggering is simple, reliable and efficient
- It is therefore the most usual method of firing the forward biased SCR
- A thyristor with forward break-over voltage (say 800 V) higher than the normal voltage (say 400V) is chosen
- This means that thyristor will remain in forward blocking state with normal working voltage across anode and cathode and with gate open
- However when turn of a thyristor required, a +ve gate voltage between gate and cathode is applied

- The forward voltage at which the device switches to on state depends on the magnitude of gate current
- Higher is the gate current lower is the forward break-over voltage
- When +ve gate current is applied, gate p layer is flooded with electrons from the cathode
- This is because cathode n layer is heavily doped as compared to gate p layer
- As the thyristor is forward biased, some of these electrons reaches junction J2
- As a result width of the depletion layer near junction J2 is reduced
- This cause the junction J2 to break down at an applied voltage lower than the forward break-over voltage V_{BO}

Turn on methods of SCR

- Once the SCR is conducting a forward current, reverse biased junction J2 no longer exist
- No gate current is required for the device to remains in on state
- Therefore if the gate current is removed, the conduction of current from anode to cathode is unaffected
- However if the gate current reduced to zero before rising the anode current attains a value, called latching current the device will turn off again
- *The latching current may be defined as the minimum value of anode current which it must attain during turn on process to maintain conduction when gate signal is removed*

- Once the thyristor is conducting, gate loses control
- The thyristor can be turned off only if the forward current falls below a low level current called holding current
- *The holding current may be defined as the minimum value of anode current below which it must fall for turning off the thyristor*
- The latching current is higher than holding current
- The latching current is associated with the turn on process and holding current with turn off process
- Usually latching current is 2 to 3 times the holding current
- In industrial applications, holding current (typically 10 m A) is almost taken as zero

dv/dt triggering

- With forward voltage across anode and cathode, the two outer junctions J1 and J3 are forward biased and inner junction J2 is reverse biased
- This reverse biased junction J2 has the characteristics of a capacitor due to charges existing across the junction
- In other words space charge exist in the depletion region near junction J2 and therefore junction J2 behaves like a capacitance
- If forward voltage is suddenly applied, a charging current through junction capacitance Cj may turn on the SCR
- Almost the entire suddenly applied forward voltage Va appears across junction J2 the charging current i_c

$$i_c = \frac{dQ}{dt} = \frac{d}{dt}(C_j.V_a) = C_j\frac{dV_a}{dt} + V_a\frac{dC_j}{dt}$$

- As the junction capacitance is almost constant, dCj/dt is zero and current ic,

$$i_c = C_j\frac{dV_a}{dt}$$

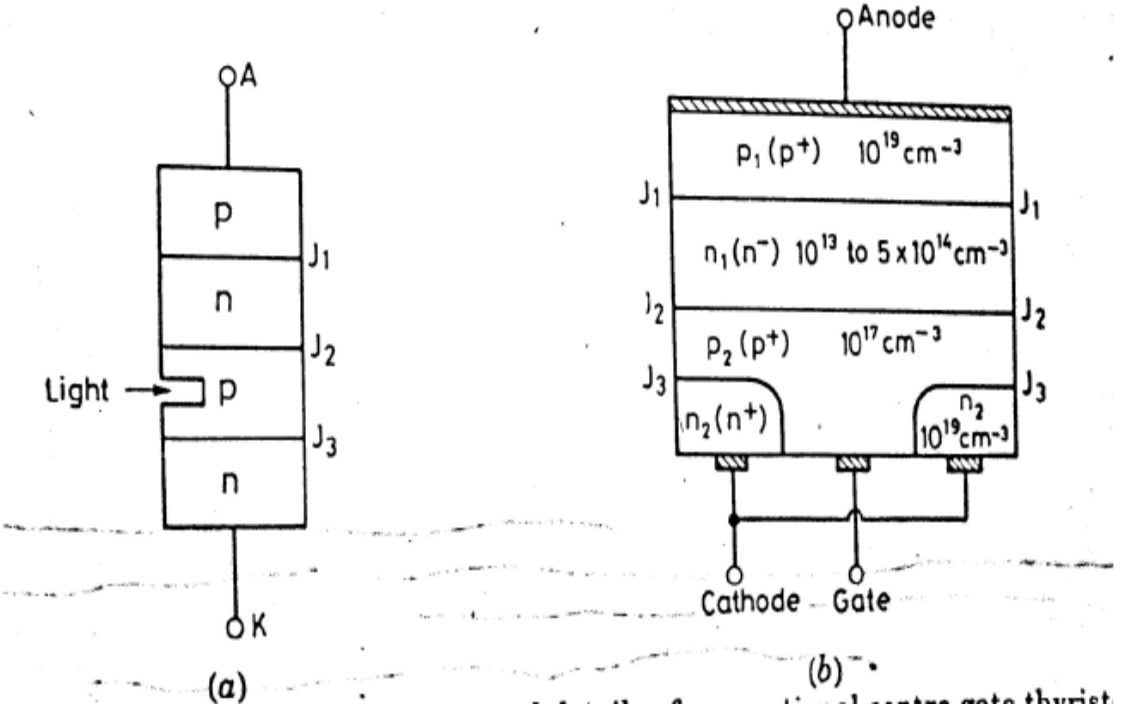
- If the rise of forward voltage dVa/dt is high, the charging current ic would be more
- This charging current plays the role of gate current and turn on the SCR even though gate signal is zero
- Note that even if Va is small, it is the arte of change of Va that plays the role of turning on the device

Temperature triggering (thermal triggering)

- During forward blocking, most of the applied voltage appears across reverse biased junction J2
- This voltage across J2, associated with leakage current, would rise the temperature of this junction
- With increase in temperature, width of depletion layer decreases
- This further leads to more leakage current and therefore more junction temperature
- With this cumulative process at some high temperature, depletion layer of reverse biased junction vanishes and the device gets turned on

Light triggering

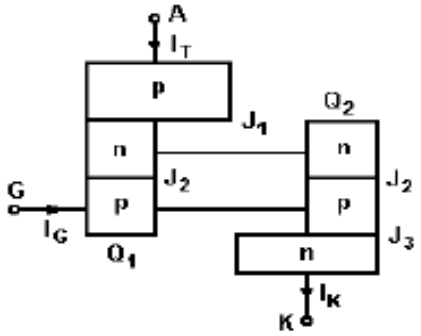
- For light triggered SCR, a recess is made in the inner p layer
- When this recess is irradiated free charge carriers are generated just like when gate signal is applied between gate and cathode



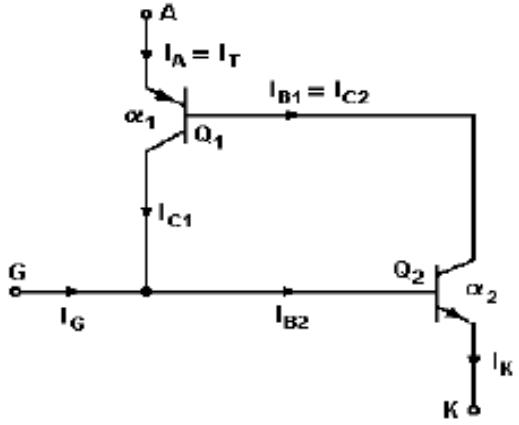
- The pulse of light of appropriate wavelength is guided by optical fibers for irradiation
- If the intensity of this light thrown on the recess exceeds a certain value, forward biased SCR is turned on
- Such a thyristor is known as light activated SCR (LASCR)
- LASCR may be triggered with a light source or with a gate signal
- Sometimes a combination of both may be used
- Light triggered SCR have now been used in high voltage direct current (HVDC) transmission system

Two transistor analogy

- The principle of thyristor operation can be explained with the use of its transistor model (or two transistor analogy)
- Two transistor model is obtained by bisecting the two middle layers along the dotted line, in tow separate halves
- Junction J1-J2 and J2-J3 can be considered to constitute pnp and npn transistors separately



(a) Basic structure



(b) Equivalent circuit

Two transistor analogy

- In the off state of a transistor, collector current Ic is related to emitter current I_E as

$$I_c = \alpha I_E + I_{CBO}$$

- Where α is the common base current gain
- I_{CBO} is the common base leakage current of collector base junction of a transistor
- For transistor Q1, emitter current IE= anode current Ia and Ic= collector current Ic1
- Therefore for Q1

$$I_{c1} = \alpha_1 I_a + I_{CBO1}$$

- Similarly for transistor Q2

$$I_{c2} = \alpha_2 I_k + I_{CBO2}$$

- The sum of two collector current is equal to the external circuit current Ia entering at anode terminal A

$$I_a = I_{c1} + I_{c2}$$

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 I_k + I_{CBO2}$$

- When gate current is applied the Ik=Ia+Ig, by substituting this

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 (I_a + I_g) + I_{CBO2}$$

$$I_a = \frac{\alpha_{2*} I_g + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

- For a silicon transistor, current gain α is very small at low emitter current
- With an increase in emitter current, α build up rapidly
- With gate Ig=0 and with thyristor forward biased, ($\alpha 1 + \alpha 2$) is very small
- Under this condition forward leakage current some what more than $I_{CBO1}+I_{CBO2}$ flows
- If by some means the emitter current of two component transistors can be increased so that $\alpha 1 + \alpha 2$ approaches unity
- As per above equation (equation for Ia) Ia tends to become infinity, thereby turning on the device

Series and parallel connection of SCR

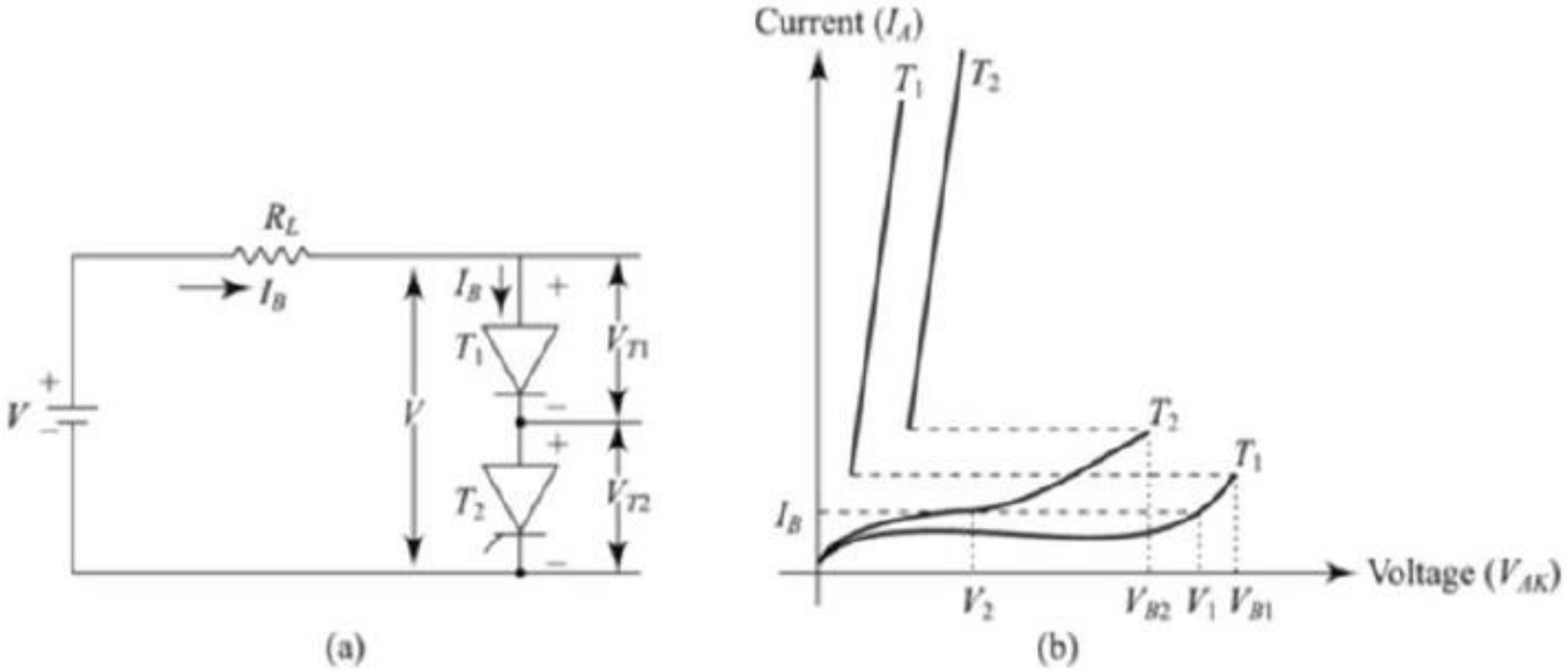
- For some industrial applications, the demand for voltage and current ratings is so high that a single SCR cannot fulfill such requirements
- In such cases *SCRs are connected in series in order to meet the H.V demand and in parallel to meet the high current demand*
- For series or parallel connected SCR it should be ensure that each SCR rating is fully utilized and the system operation is satisfactory
- String efficiency is a term that is used for measuring the degree of utilization of SCRs in a string

$$string\ efficiency = \frac{actual\ voltage\ /current\ rating\ of\ the\ whole\ string}{[individual\ volatge/current\ rating\ of\ \ oneSCR]\ [Number\ of\ SCR\ in\ a\ string\ ]}$$

- In practice this ratio is less than one
- For obtaining highest possible string efficiency, the SCRs connected in series / parallel string must have identical V-I characteristics
- As SCRs of same ratings and specifications do not have identical characteristics, unequal voltage/ current sharing is bound to occur for all SCRs in a string
- As a consequence string efficiency can never be equal to one
- However unequal voltage/ current sharing by the SCRs in a string can be minimized to a great extend by using external equalizing circuits
- Even this equalizing circuits, the efficiency is less than unity

- For a given system if one extra unit is added to the series / parallel string, the voltage / current shared by each device would become lower than its normal rating
- The use of voltage / current shared by each device would become lower than its normal rating
- The use of this extra unit will certainly improve the reliability of the string though at an increased cost
- A measure of the reliability of the string is given by a factor called DRF – derating factor
- DRF=1- string efficiency

Series operation



(a) Series connection of thyristors T_1 and T_2 (b) V-I characteristics of thyristors T_1 and T_2

Series operation

- When system voltage is more than the voltage rating of a single thyristor, SCRs are connected in series in a string
- As stated before, these SCRs should have their V-I characteristics as close as possible
- Consider 2 SCR with their V-I characteristics
- For SCR1 leakage resistance is high (=V1/Io)
- For SCR2 it is low (V2/Io)
- For the same leakage current Io in the series connected SCRs, SCR1 support rated voltage whereas SCR2 support voltage V2<V1
- Two SCR can support a maximum voltage of V1+V2 and not the rated blocking voltage 2V1

- The string efficiency for two series connected SCRs

$$\frac{V_1 + V_2}{2V_1} = \frac{1}{2}\left(1 + \frac{V_2}{V_1}\right)$$

- A uniform voltage distribution in steady state can be achieved by connecting a suitable resistance across each SCR such that each parallel combination has the same resistance
- This will require different values of resistance for each SCR which is a difficult proposition
- A more practical way of obtaining a reasonably uniform voltage distribution during steady state working of series connected SCR is to connect the same value of shunt resistance R across each SCR
- This shunt resistance R is called the static equalizing circuit

- Let there be n_s thyristors in the string
- The off state current of thyristor T1 be ID1 and that of other thyristor are equal such that $I_{D2} = I_{D3} = I_{Dn}$ and $I_{D1} < I_{D2}$
- Because thyristor T1 has the least off state current T1 shares higher voltage
- If I1 is the current through the resistor R across T1 and the current through other resistors are equal so that I2=I3=In
- The off –state current spread is

$$\Delta I_D = I_D - I_{D1} = I_T - I_2 - I_T + I_1 = I_1 - I_2 \text{ or } I_2 = I_1 - \Delta I_D$$

- The voltage across T1 is $V_{D1} = R*I1$
- Using Kirchhoff's voltage law

$$V_s = V_{D1} + (n_s - 1)I_2R = V_{D1} + (n_s - 1)(I_1 - \Delta I_D)R$$

$$= V_{D1} + (n_s - 1)I_1R - (n_s - 1)\,R\Delta I_D$$

$$= n_sV_{D1} - (n_s - 1)R\Delta I_D$$

- Solving above equation for the voltage V_{D1}

$$V_{D1} = \frac{V_s + (n_s - 1)R\Delta I_D}{n_s}$$

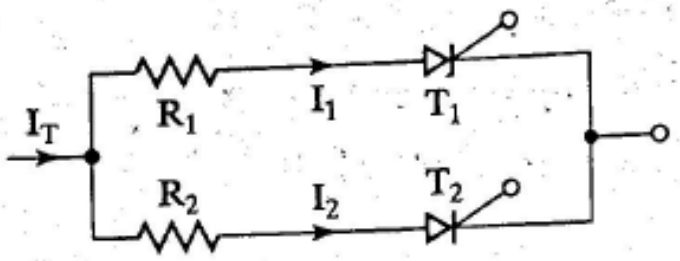
- A derating factor that is normally used to increase the reliability of the string is defined as the

$$DRF = 1 - \frac{V_s}{n_sV_{DS(\max)}}$$

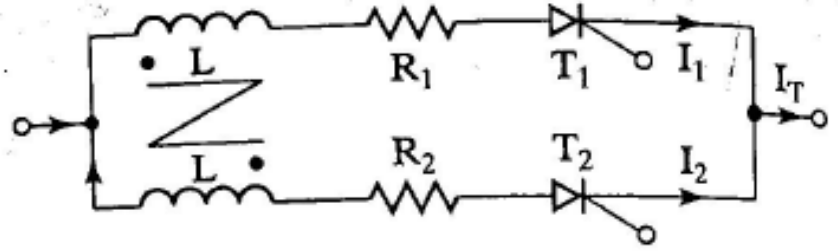
Parallel operation

- When thyristors are connected in parallel, the load current is not shared equally due to different in their characteristics
- If a thyristor carries more current than that of the others, its power dissipation increases thereby increasing the junction temperature and decreasing the internal resistance
- This in turn increases its current sharing and may damage the thyristor
- This internal runaway may be avoided by having a common het sink , so that all units operate at same temperature
- A small resistance may be connected in series with each thyristor to force equal current sharing

- But there may be considerable power loss in the series resistance
- A common approach for the current sharing of thyristors is to use magnetically coupled inductors
- If the current through thyristor T1 increases a voltage of opposite polarity can be induced in the winding of thyristor T2 and the impedance through the path of T2 can be reduced, thereby increasing the current flow through T2



(a) Static current sharing

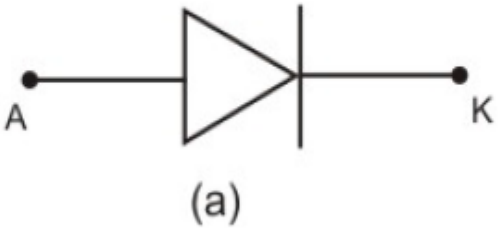


(b) Dynamic current sharing

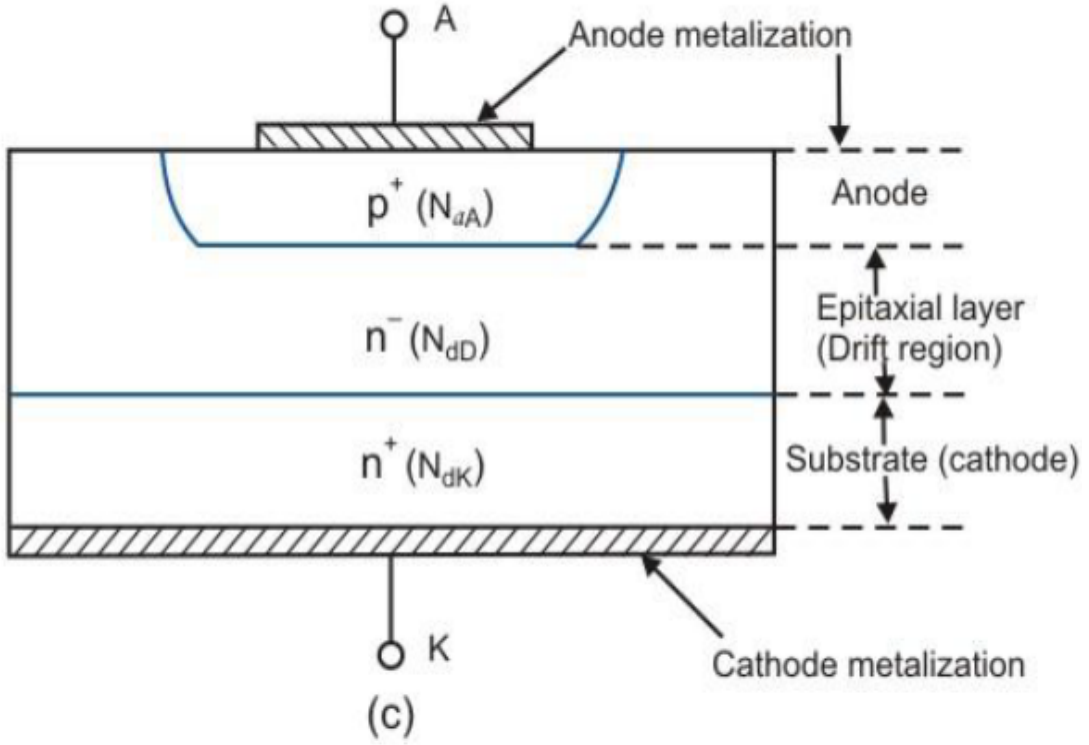
Power semiconductor diode

- Power semiconductor diode is the "power level" counter part of the "low power signal diodes"
- These power devices, however, are required to carry up to several KA of current under forward bias condition and block up to several KV under reverse biased condition.
- That is the construction of power diodes arises from the need to make them suitable for high-voltage and high-current applications.
- These extreme requirements call for important structural changes in a power diode which significantly affect their operating characteristics.
- The practical realization and resulting structure of a power diode is shown

Power semiconductor diode – structure



(a)



(c)

Circuit symbol, photograph and cross sectional view of a power diode

- It consist of heavily doped n+ substrate
- On this substrate, a lightly doped n- layer is epitexially grown
- Now a heavily doped p+ layer is diffused into n- layer to form the anode of the power diode
- This shows that n- layer is the basic structural feature not found in signal diodes
- The function of n- layer is to absorb the depletion layer of the reverse biased p+ n- junction J1
- The breakdown voltage needed in a power diode governs the thickness of n- layer
- Greater the breakdown voltage, more the n- layer thickness

- The drawback of n- layer is to add significant ohmic resistance to the diode when it is conducting a forward current
- This leads to large power dissipation in the diode
- So proper cooling arrangements in large diode ratings are essential
- Circuit symbol of a power diode is same as that of a signal diode

Power semiconductor diode - Chara.

- Power diode is a two terminal, p-n semiconductor device
- The two terminals of diode are called, anode and cathode
- The two important characteristics of diode are

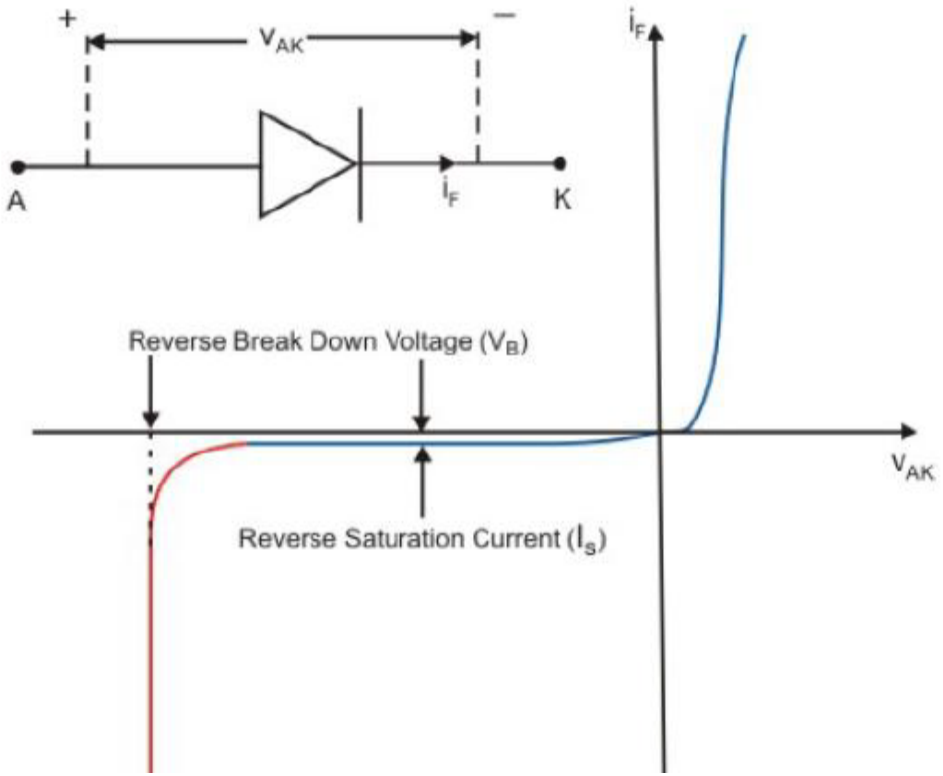
    1) Diode V-I characteristics

    2) Diode reverse recovery characteristics

Diode V-I characteristics

- When anode is positive w.r.t cathode, diode is said to be forward biased
- With increase of the source voltage Vs from zero value, initially diode current is zero
- From Vs =0 to cut in voltage, the forward diode current is very small
- *Cut in voltage is also known as, threshold voltage or turn on voltage*
- Beyond cut in voltage, the diode current rises rapidly and the diode is said to conduct

- For silicon diode, the cut in voltage is around 0.7 V
- When diode conducts, there is a forward voltage drop of the order of 0.8 to 1 V

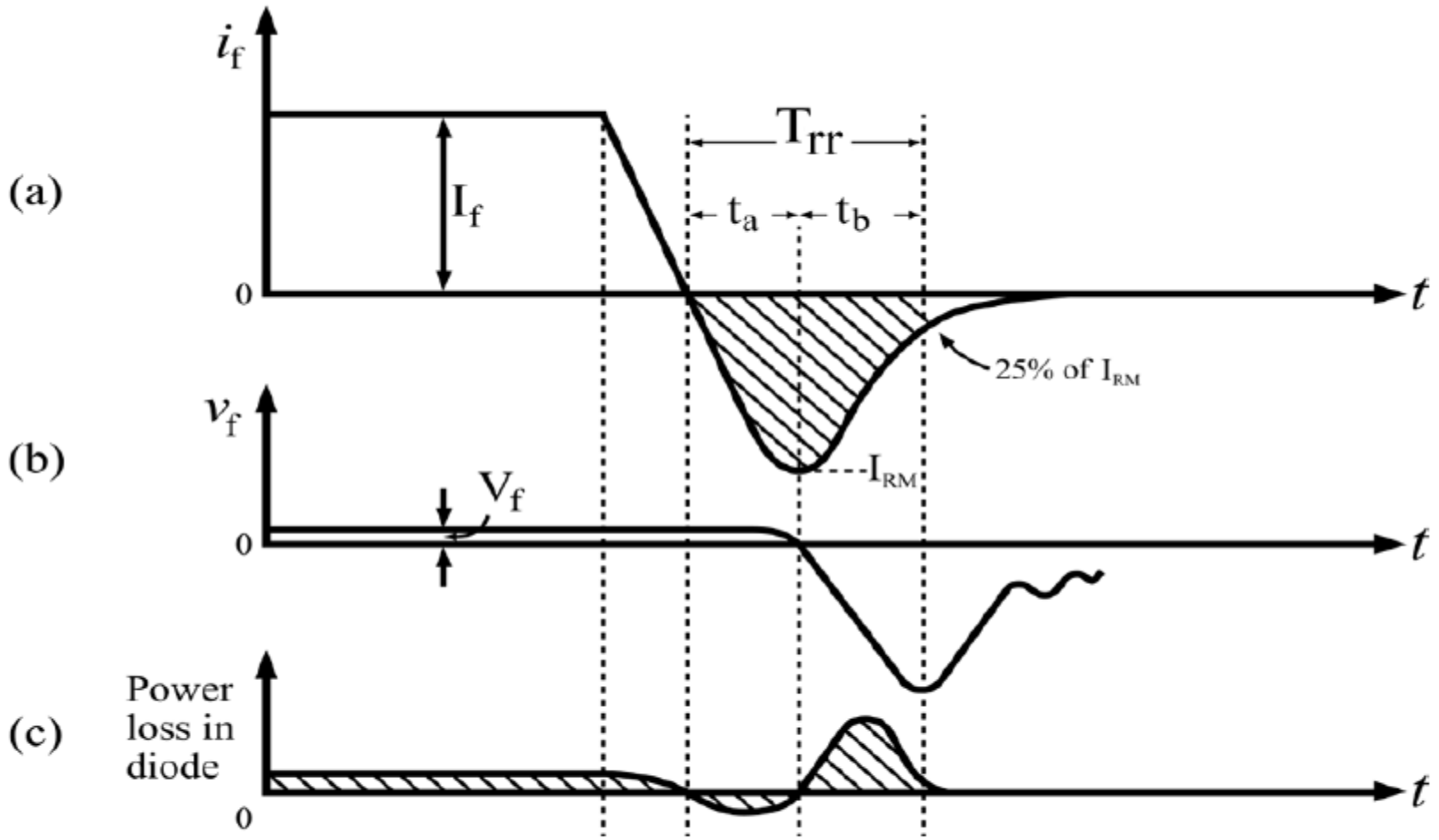


- When cathode is positive w.r.t anode, the diode is said to be reverse biased
- In the reverse biased condition a small reverse current called leakage current of the order of microamperes or mill amperes flows
- The leakage current is almost independent of the magnitude of reverse voltage until this voltage reaches breakdown voltage
- At this reverse breakdown, voltage remains almost constant but reverse current becomes quite high, limited only by the external circuit resistance
- A large reverse breakdown voltage, associated with high reverse current leads to excessive power loss that may destroy the diode

- This shows that reverse breakdown of a power diode must be avoided by operating it below the specific peak reverse repetitive voltage V_{RRM}
- For an ideal diode, the voltage drop across conducting diode is zero and V_{RRM} is infinite
- Diode manufactures also indicate the value of peak inverse voltage (PIV) of a diode
- This is the *largest reverse voltage to which a diode may be subjected during its working*
- The power diodes are available with forward current rating of 1A to several thousands of ampere with reverse voltage rating of 50V to 5000V or more

Diode reverse recovery characteristics

- After the forward diode current decays to zero, the diode continues to conduct in the reverse direction because of the presence of stored charges in the depletion region and the semiconductor layers
- The reverse current flows for a time called reverse recovery time trr
- The diode regain its blocking capability until reverse recovery current decays to zero
- Is defined as *the time between the instant forward diode current becomes zero and the instant reverse recovery current decays to 25% of its reverse peak value* I_{RM}



Reverse recovery characteristics

- The reverse recovery time is composed of two segments time ta and tb, i.e. trr=ta+tb
- Time ta is the time between zero crossing of forward current and peak reverse current I_{RM}
- During ta, charge stored in depletion layer is removed
- tb- is measured from the instant of reverse peak value I_{RM} to the instant when $0.25I_{RM}$ is reached
- During tb charge from the semiconductor layer is removed
- The shaded area represent the stored charge, or reverse recovery charge Q_R which must be removed during the reverse recovery time trr

- The ratio tb/ta is called the softness factor or S - factor
- Its usual value is unity and this indicate low oscillatory reverse recovery process
- A diode with S-factor unity is called soft-recovery diode
- And a diode with S factor <1 is called snappy recovery diode or fast recovery diode
- The peak inverse current can be expressed as

$$I_{RM} = t_a \frac{di}{dt}$$

$$Q_R = \frac{1}{2} I_{RM} t_{rr} \qquad I_{RM} = \frac{2Q_R}{t_{rr}}$$

- If trr=ta

$$I_{RM} = t_{rr}\frac{di}{dt} \qquad t_{rr}\frac{di}{dt} = \frac{2Q_R}{t_{rr}}$$

$$t_{rr} = \left[\frac{2Q_R}{\left(di/dt\right)}\right]^{1/2}$$

- With ta=trr, we get

$$I_{RM} = t_{rr}\frac{di}{dt} = \left[\frac{2Q_R}{\left(di/dt\right)}\right]^{1/2} \cdot \frac{di}{dt}$$

$$= \left[2Q_R\left(\frac{di}{dt}\right)\right]^{1/2}$$

Power semiconductor diode- Types

General purpose diode

- High reverse recovery time, order of 25 micro sec
- Current rating from 1A to several thousands of ampere
- Voltage rating – 5V to 5kV
- Application – battery charging, electric traction, electroplating, welding, UPS etc..

Fast-recovery diode

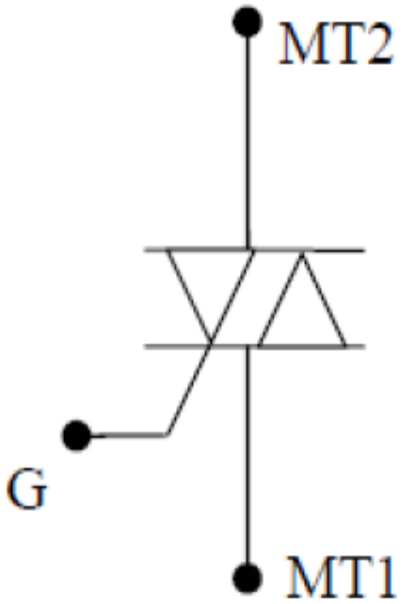
- Low reverse recovery time of about 5 micro sec
- Application – chopper, commutation circuit, SMPS, induction heating etc…
- Current rating from 1A to several thousands of ampere
- Voltage rating – 50V to 3kV

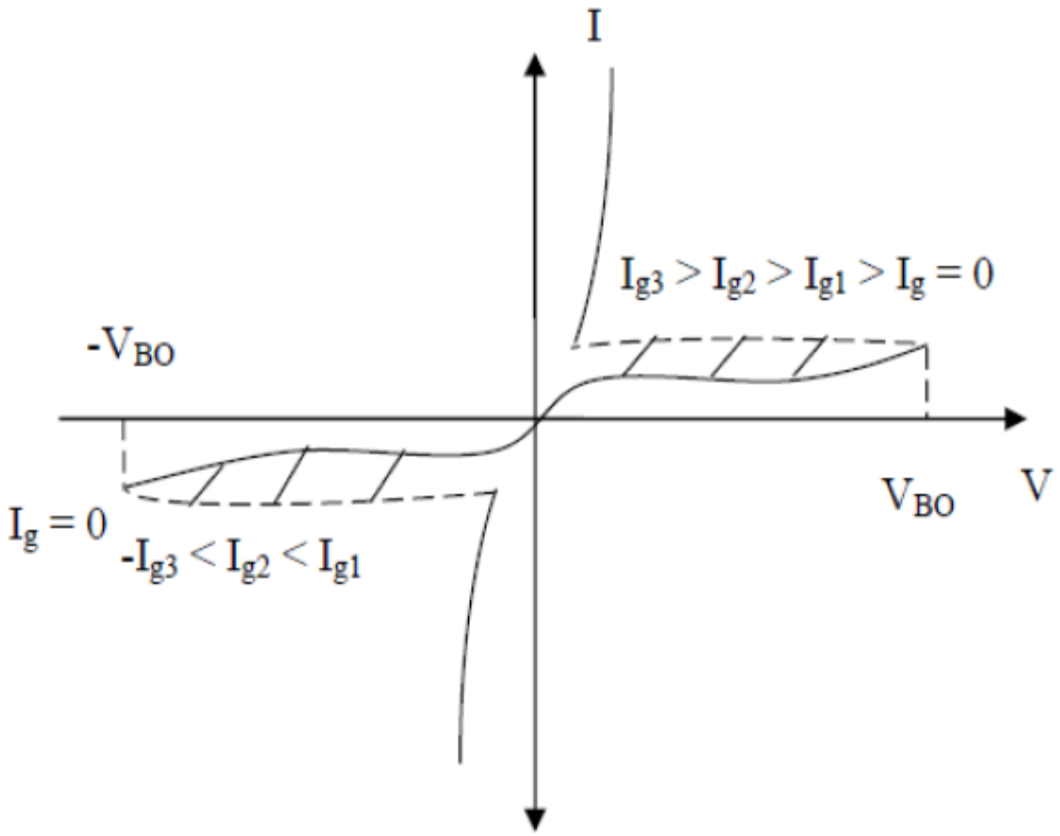
Schottky diode

- Use metal-to-semiconductor junction for rectification
- The metal is usually aluminum
- Low cut in voltage
- Higher reverse leakage current
- Higher operating frequency
- Reverse Voltage rating – 100V
- Forward current rating – 1A to 300A
- Applications – high frequency instrumentation, switching power supplies

TRIAC

- An SCR is a unidirectional device an it can conduct from anode to cathode only and not from cathode to anode
- A TRIAC can conduct in both the directions
- TRIAC – *bidirectional thyristor with three terminals*
- Extensively used for the control of power in ac circuits (residential lamp dimmers, heater control, speed control of small single phase series and IM)
- The word derived form combing the capital letters from the word TRIode and AC
- When in operation, a *TRIAC is equivalent to two SCRs connected in anti-parallel*
- The circuit symbol and characteristics are shown


MT2
G
MT1

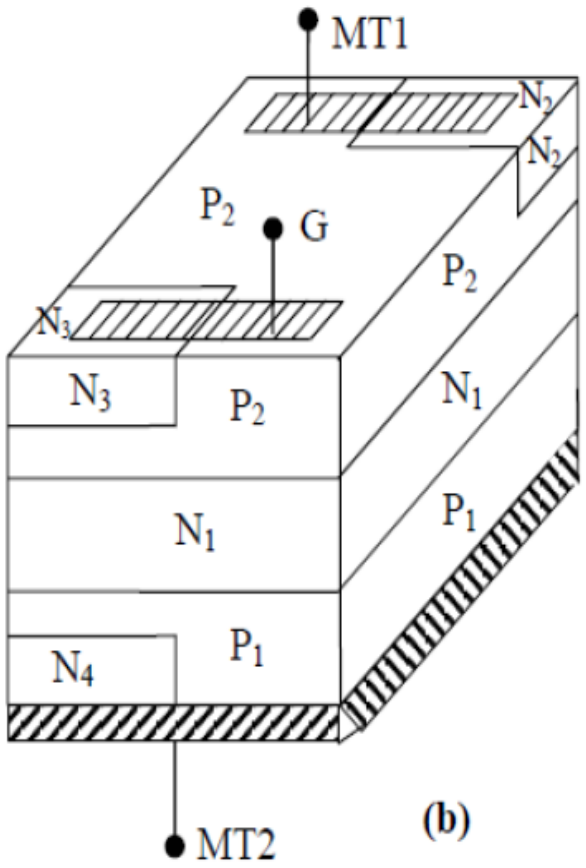

I
$I_{g3} > I_{g2} > I_{g1} > I_g = 0$
$-V_{BO}$
V_{BO}
V
$I_g = 0$
$-I_{g3} < I_{g2} < I_{g1}$

- As TRIAC can conduct in both the direction, the terms anode and cathode are not applicable to TRIAC
- Its three terminal are usually designated as

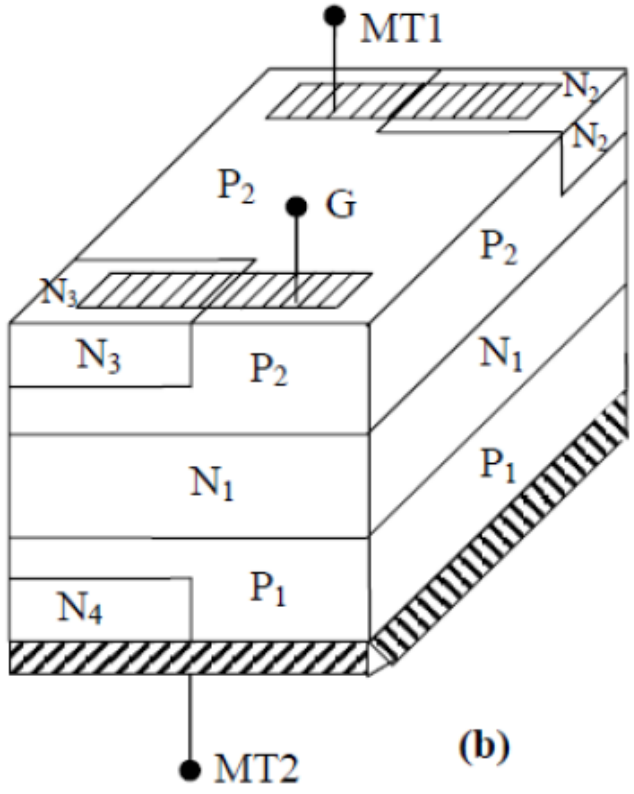
  MT1 – Main Terminal 1

  MT2 – Main Terminal 2

  G - Gate
- Cross sectional view of TRIAC showing all the layers and junction is shown



- The gate G is near terminal MT1
- The cross hatched strip shows that G is connected to N3 as well as P2
- MT1 is connected to P2 and N2
- MT2 is connected to P1 and N4



- Since TRIAC is a bidirectional device and can have its terminals at various combinations of +ve and –ve voltages, there are 4 possible electrode potential combinations as given below

    1) MT2 is +ve w.r.t MT1, G +ve w.r.t MT1
    2) MT2 is +ve w.r.t MT1, G -ve w.r.t MT1
    3) MT2 is -ve w.r.t MT1, G -ve w.r.t MT1
    4) MT2 is -ve w.r.t MT1, G +ve w.r.t MT1

- Trigeering sensitivity is highest – for combination 1 &3
- For bidirectional control and uniform gate trigger – 2 & 3 used
- 4 usually avoided

Mode – 1(MT2 is +ve w.r.t MT1, G +ve w.r.t MT1)

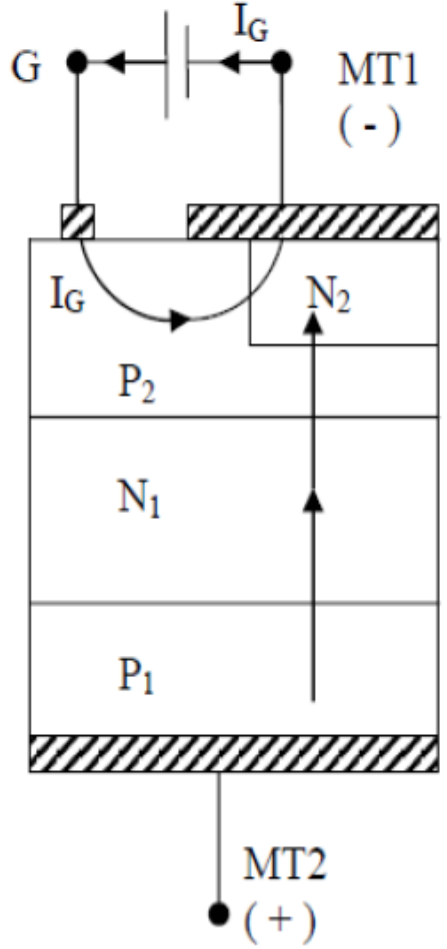
- When MT2 is +ve w.r.t MT1 – junction P1N1, P2N2 are forward biased
- Junction N1P2 reverse biased
- When G is +ve w.r.t MT1-

  gate current flows mainly through P2N2
- When gate current has injected sufficient

  charges into P2 layer, reverse biased junction

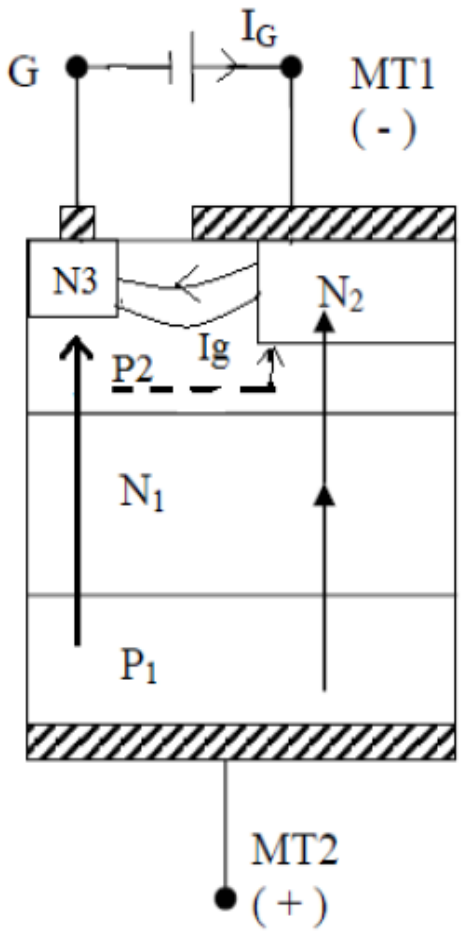
  N1P2 breaks down
- As a result TRIAC starts conducting through -

  P1N1P2N2
- TRIAC operates in the first quadrant



Mode – 2 (MT2 is +ve w.r.t MT1, G -ve w.r.t MT1)

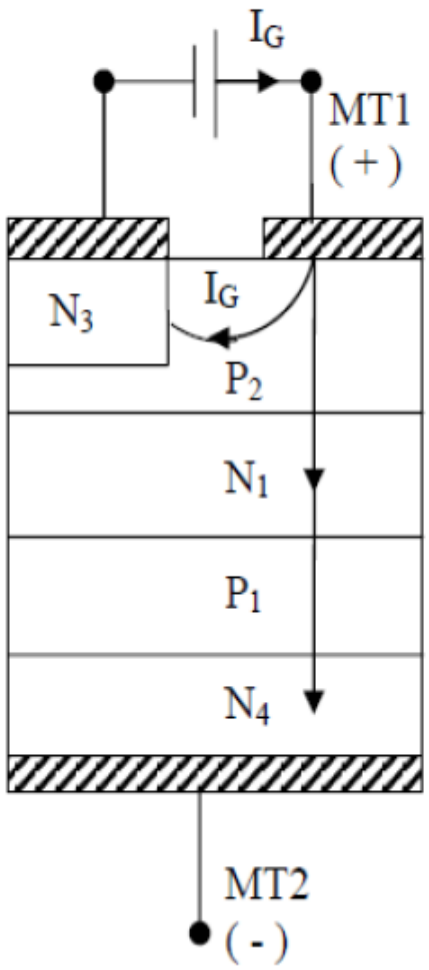
- When G is –ve w.r.t MT1, gate current flows through P2N3
- N1P2 – forward biased
- Conduction through – P1N1P2N3
- With the above conduction, voltage drop across this path falls but P2N3 rises towards MT2
- A potential gradient exist across P2
- Left hand region become higher potential than right hand region
- Current (shown in dotted line) established



- As a result right hand portion P1N1P2N2 begins to conduct
- The device structure P1N1P2N3 regarded as – pilot SCR
- P1N1P2N2- main SCR
- Device with MT2 +ve and G –ve is less sensitive
- Therefore more gate current is required

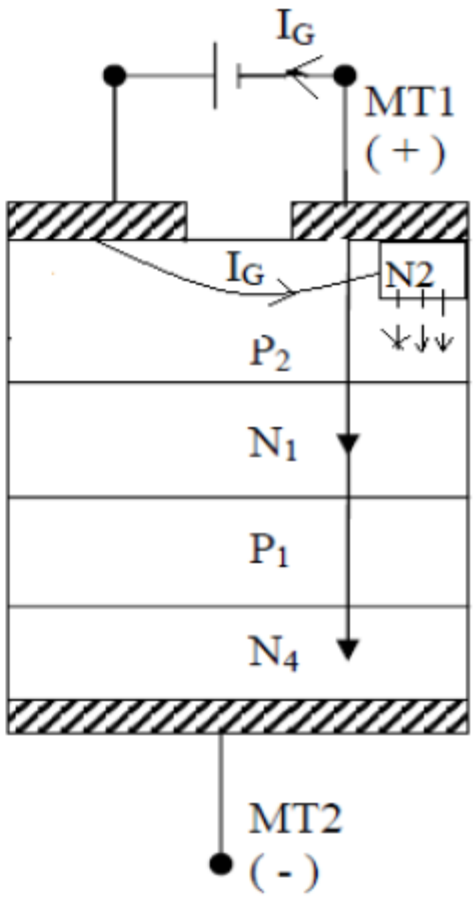
Mode 3 (MT2 is -ve w.r.t MT1, G -ve w.r.t MT1)

- N3 act as a remote gate
- Gate current flows from – P2 to N3
- Reverse biased junction – N1P1 is broken
- Finally P2N1P1N4 is turned on completely
- Operation is in 3rd quadrant
- Device is more sensitive under this condition



Mode 4 (MT2 is -ve w.r.t MT1, G +ve w.r.t MT1)

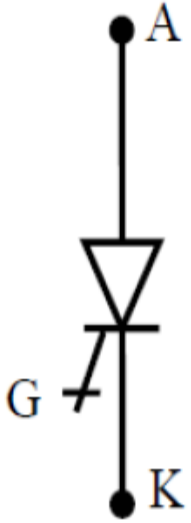
- Gate current forward biases junction – P2N2
- N2 inject electrons into P2 layer (shown by dotted arrows)
- As a result reverse biased junction N1P1 breaks down
- The structure P2N1P1N4 is completely turned on
- Current after turn on is limited by external load
- Device is less sensitive
- Operation is in 3rd quadrant



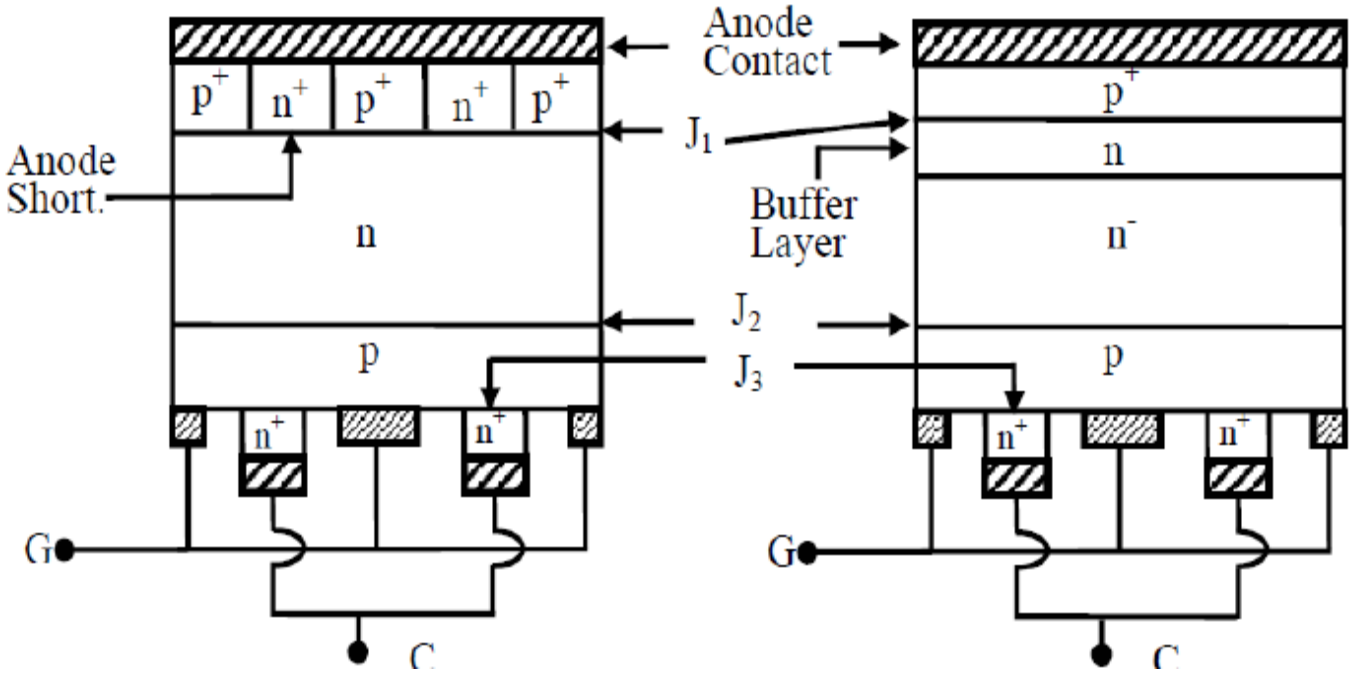
GTO (Gate Turn Off thyristor)

- Conventional thyristor (CTs) are nearly ideal switches for their use in power electronic application
- These can be easily turned on by positive gate current
- Once in the on state, gate loses control
- CTs can now be turned off by expensive and bulky commutation circuitry
- This shortcoming of thyristors limit their use up to about 1KHz applications
- These drawbacks in thyristors has led to the development of GTOs

- GTO is a more versatile power semiconductor device
- Like a CT but with added features in it
- Can be easily turned off by a –ve gate pulse of appropriate amplitude
- GTO – pnpn device that can be turned on by a +ve gate current and turned off by a –ve gate current at its gate cathode terminal
- Self turn off capability of GTO makes it the most suitable device for inverter and chopper circuit



- pn pn three terminal device with Anode (A) cathode (K) and gate (G)
- Four layers are – p+ n p+ n+
- Anode is made up of n+ type diffused into p+ layer
- anode shorted GTO and buffer layer GTO structure shown below

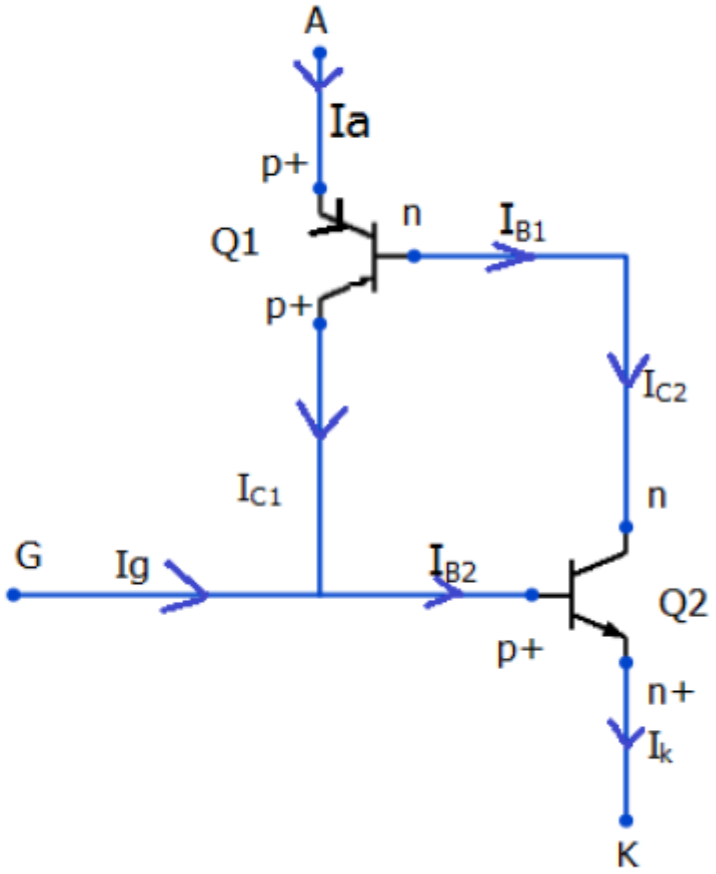


GTO – Turn on process

- Turned on by applying a +ve gate current
- As GTO is forward biased, regeneration process starts as in a CT
- Current gains, $\alpha 1$, $\alpha 2$ begins to rise
- When $\alpha 1 + \alpha 2 = 1$, saturation level is reached and GTO is turned on
- The anode current Ia is then limited by load impedance

GTO – Turn off process

- Two transistor model is analyzed for understanding the turn off process in a GTO
- $I_{c2} = \beta_2 . I_{B2}$
- $I_{c1} = \beta_1 . I_{B1}$
- $I_{c1} = \alpha_1 . I_{E1}$
- $I_{c2} = \alpha_2 . I_{E2}$
- As stated above, for initiating the turn off process in GTO a –ve gate current is applied across gate cathode terminal



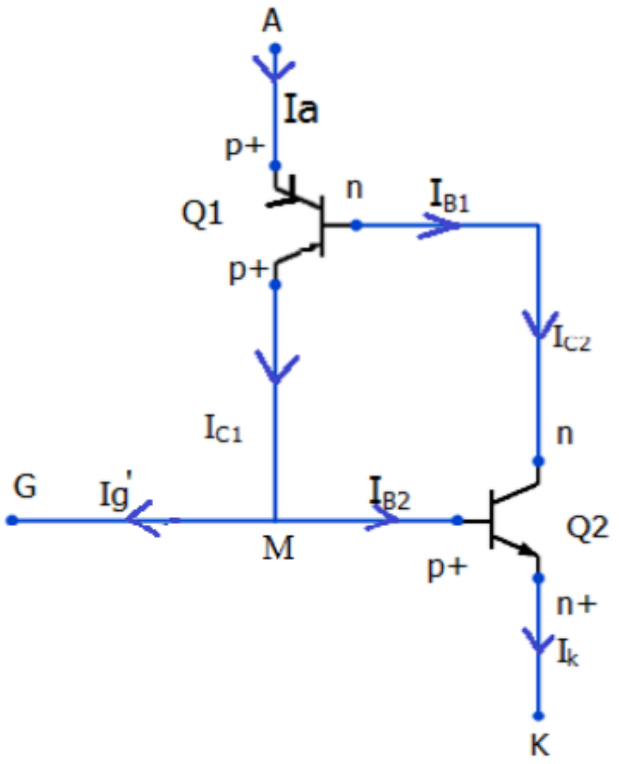
- Now KCL at node M gives,

$$I_{C1} - I_g' - I_{B2} = 0$$

$$I_{B2} = I_{C1} - I_g' = \alpha_1 . I_a - I_g'$$

$$I_a = I_{C1} + I_{C2}$$

$$I_{C2} = I_a - I_{C1} = (1 - \alpha_1) . I_a$$



- When saturation in Q2 has occurred

$$I_{B2} = (I_{C2} / \beta_2)$$

- For initiating the turn off process,

  Q2 must be brought out of saturation

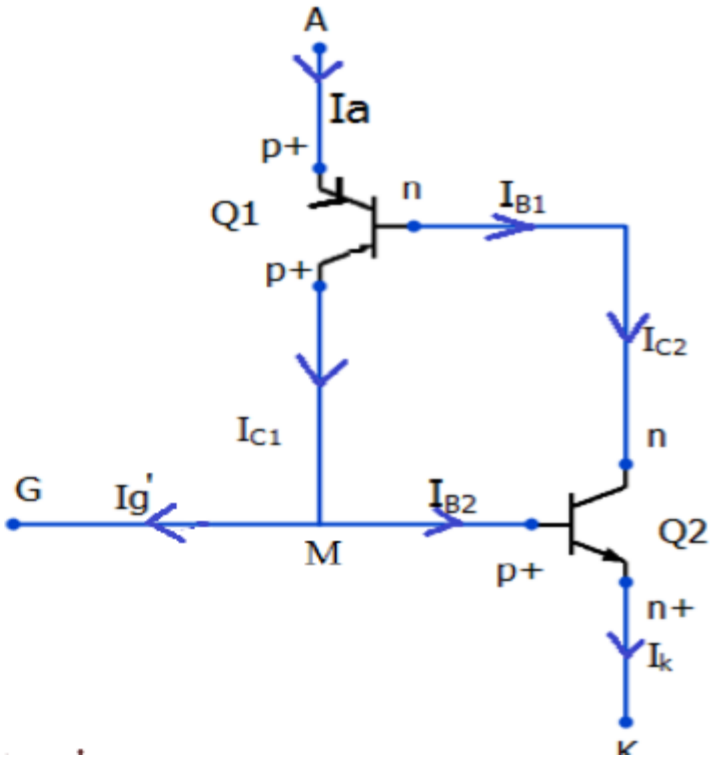
- This can be accomplished only if I_{B2} is made less than I_{C2} / β_2

- When $I_{B2} < (I_{c2}/\beta_2)$, Q2 would shift to active region and regenerative action would eventually turn off the GTO
- The turn off gain is defined as the ratio of anode current Ia to gate current Ig' needed to turn off the GTO
- Turn – off gain $\beta_{off} = I_a / I_g' = \alpha_2/(\alpha_1+\alpha_2-1)$

Turn off action of GTO

- Ia=Ik and Ig' more than Ik
- When –ve gate current Ig' flows between gate – cathode terminals net base current (I_{B2}- Ig') is reversed
- Excess carriers are drawn from base p+ region of Q2 and collector current I_{C1} of Q1 is diverted into the external gate circuit

- This remove base drive of transistor Q2
- This further removes base current I_{B1} of transistor Q1
- And the GTO is eventually turned off
- Low value of negative gate current requires, low value of $\alpha 1$ and high value of $\alpha 2$



Applications of GTO

- High performance drive system such as field oriented control scheme used in rolling mills, robotics and machine tools
- Traction purpose because of their lighter weight
- Adjustable frequency inverter drives
- at present GTO with ratings up to 5000 V and 3000 A are available

IGBT

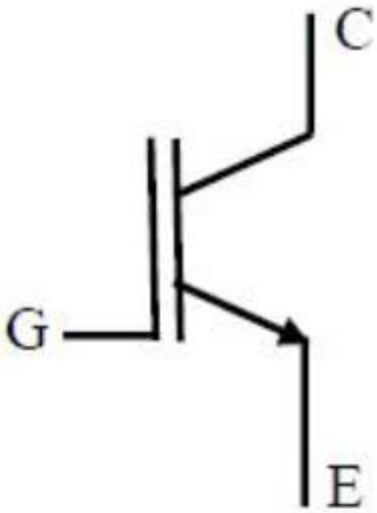
- Developed by combining the best qualities of both BJT and MOSFET
- Thus an IGBT posses high input impedance like MOSFET and has low on state power loss as in BJT
- Free from secondary breakdown problem
- Also known as

  Metal Oxide Insulated Gate Transistor (MOSIGT)

  Conductively Modulated Field Effect Transistor (COMFET)

  Gain Modulated FET (GEMFET)

  Insulted Gate Transistor (IGT)

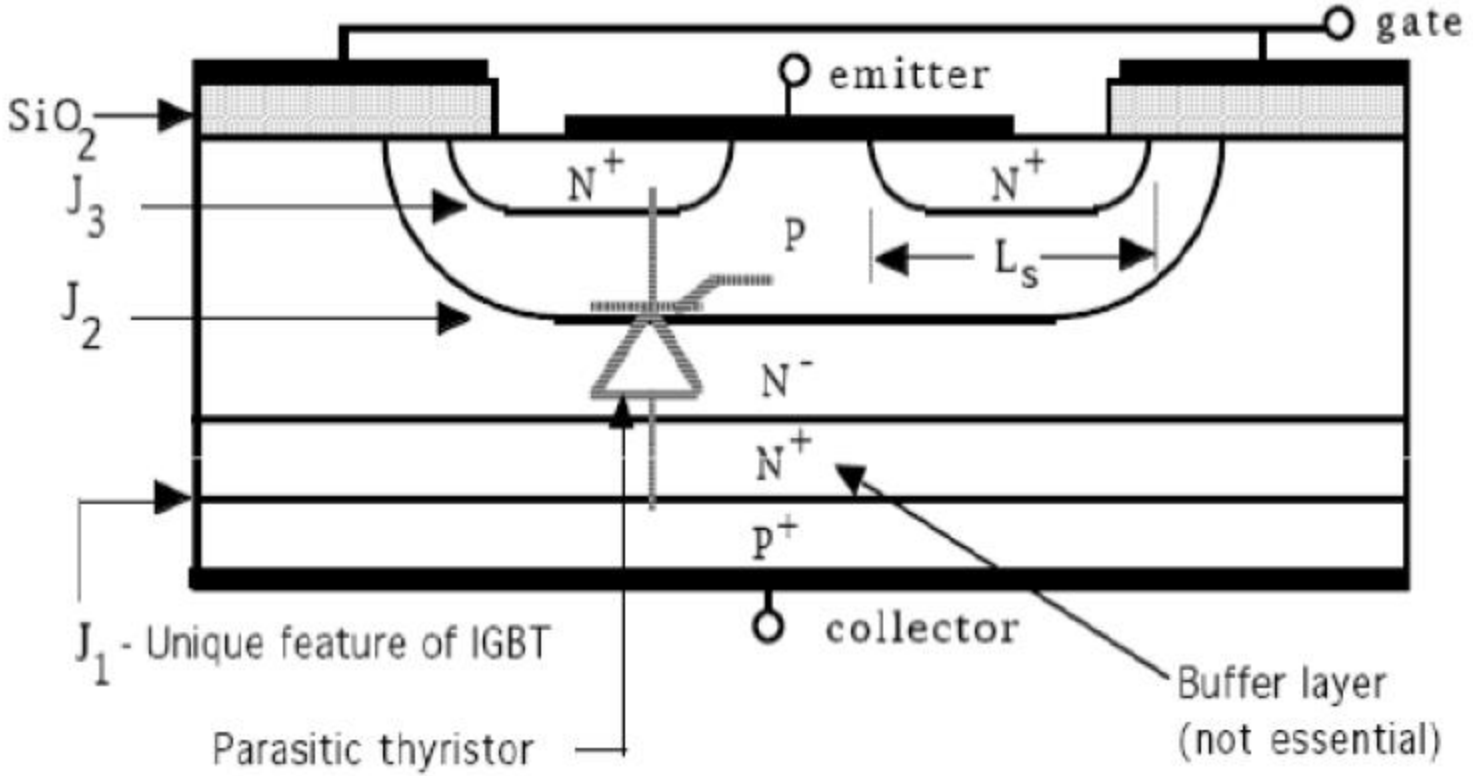


(a)

(b)

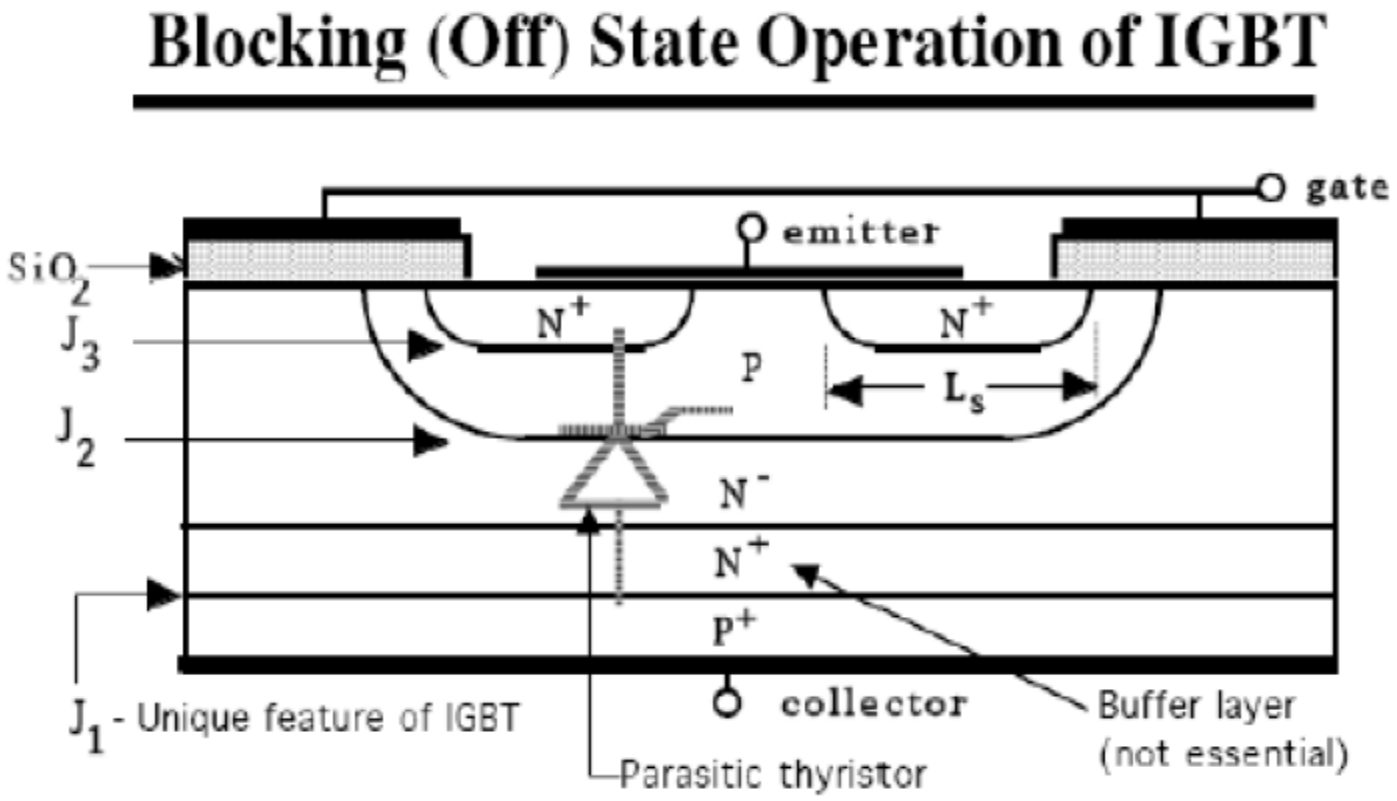
Circuit symbol of an IGBT.
(a) Circuit symbol.
(b) Photograph.

Basic structure of an IGBT



- Body region and emitter is shorted to minimize possible turn on of the thyristor.
- n+ buffer layer is between P+ and n- drift layer, is not essential for the operation of the IGBT.
- (IGBT with buffer layer is called punch- through type, PT-IGBT's and without buffer layer is called non-punch through type, NPT- IGBT's)
- Buffer layer improves the operation of IGBT.

Blocking state operation



- Blocking state operation - $V_{GE} < V_{GE(th)}$

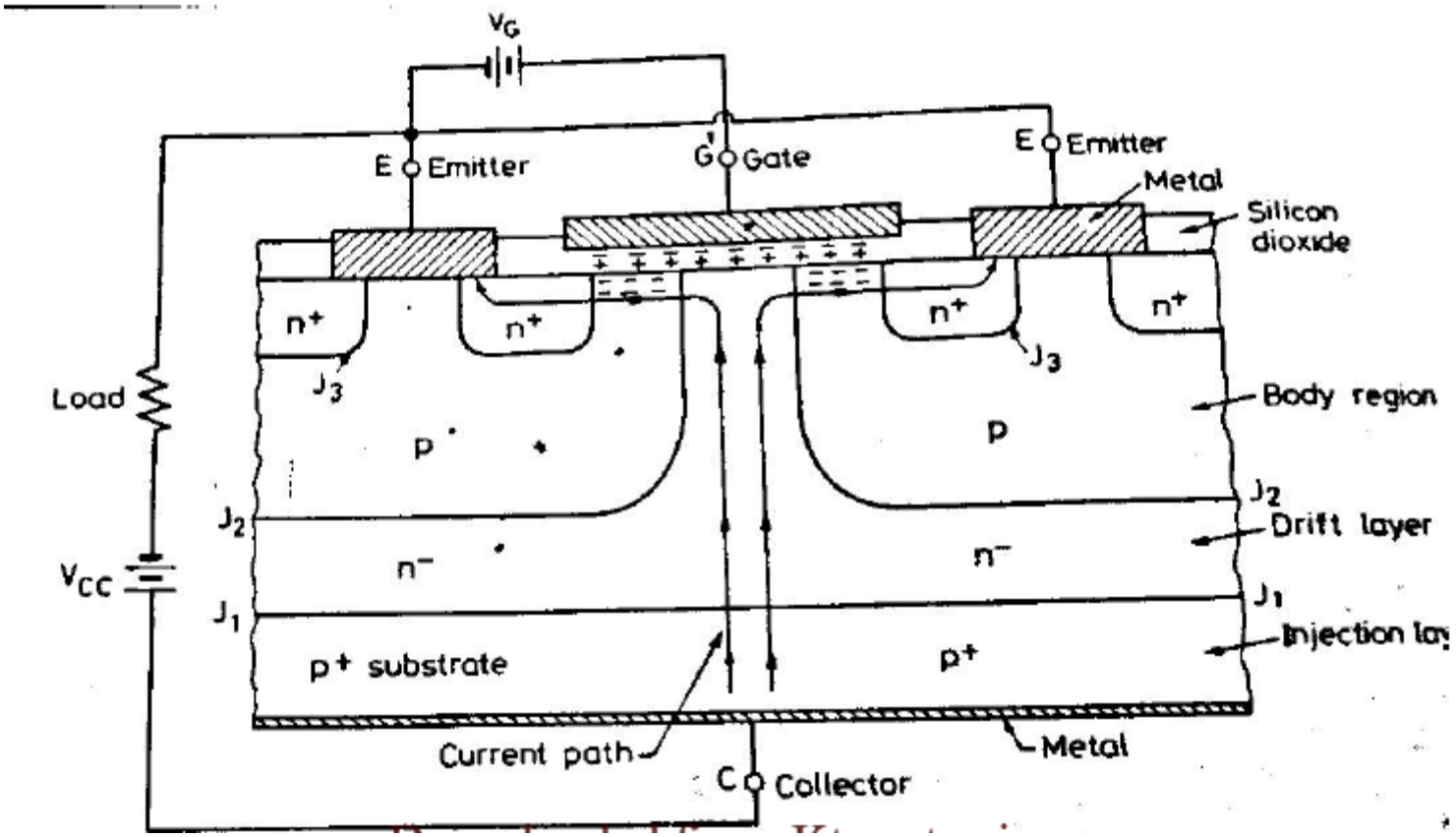
- Applied Collector emitter voltage is dropped across junction J2 and only very small leakage current flows.
- Depletion region of the J2 junction extends principally into the n- drift region (since P type body region is more doped than n- drift region)
- Thickness of drift region is large enough to accommodate depletion layer so that depletion layer boundary does not touch P+ layer. So it can block reverse voltage (magnitude same as forward voltage)
- This type of IGBT is known as symmetrical IGBT or non-punch through IGBT.

- This reverse voltage blocking capability is useful in some ac circuit applications.
- If thickness of drift region is reduced , depletion layer may touch P+ . To avoid that we keep a buffer layer, n+ layer.
- This type of structure is called anti symmetric or punch through IGBT .
- Shorter drift region means lower on-state losses.
- Presence of buffer layer reverse voltage capability quite low.

On state operation

- Gate – emitter voltage increases to more than threshold value , an inversion layer is formed beneath the gate of IGBT.
- This inversion layer shorts the n- drift region to the n+ source region exactly as in the MOSFET.
- An electron current flows through this inversion layer which in turn causes substantial hole injection from the P+ drain contact layer in to n- drift region as shown in figure.
- The injected holes move across the drift region by both drift and diffusion, taking a variety of path, and reach the p type body region that surrounds the n+ source region.

- As soon as the holes are in the p type body region, their space charge attracts electrons from the emitter metallization that contacts the body region, and the excess holes are quickly recombined.



Comparison of IGBT with MOSFET

IGBT

- Three terminal called, gate, emitter and collector
- High input impedance
- Voltage controlled device
- Can designed for higher voltage rating than PMOSFET

MOSFET

- Three terminal called, gate, source and drain
- High input impedance
- Voltage controlled device
- On state voltage drop and losses rises rapidly than IGBT with rise in temperature

Comparison between GTO and Thyristor

Disadvantages

- Magnitude of latching and holding current is more
- On state voltage drop and associated loss is more
- Triggering gate current required is high
- Gate drive circuit losses are more
- Reverse voltage locking capability is less than forward voltage blocking capability

Advantages

- Faster switching speed
- Surge current capability is comparable with an SCR
- More di/dt rating at turn on
- GTO circuit configuration has low size and weight
- Higher efficiency
- Reduced acoustical and electromagnetic noise due to elimination of commutation chokes

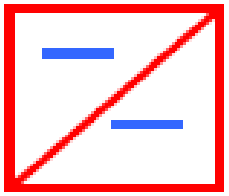
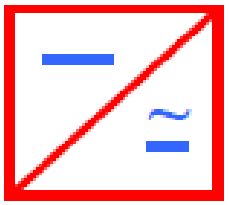
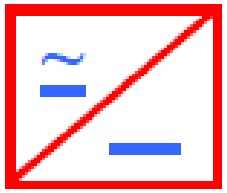
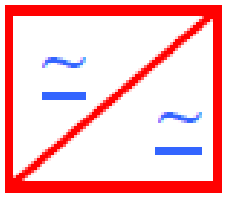
Power MOSFET – Comparison with BJT

BJT

- Bipolar
- Input impedance low
- Higher switching losses
- Current controlled device
- -ve temperature coefficient
- Hot spot and secondary breakdown occur in BJT
- Available with rating up to 1200 V, 800 A

MOSFET

- Uni-polar device
- High input impedance
- Lower switching losses and conduction losses
- voltage controlled device
- +ve temperature coefficient
- Secondary breakdown does not occur
- High voltage rating, more conduction loss
- 500 V, 140 A

CONVERSION FROM/TO	NAME	FUNCTION	SYMBOL
DC to DC	Chopper	Constant to variable DC or variable to constant DC	
DC to AC	Inverter	DC to AC of desired voltage and frequency	
AC to DC	Rectifier	AC to unipolar (DC) current	
AC to AC	Cycloconverter, AC-PAC, Matrix converter	AC of desired frequency and/or magnitude from generally line AC	

MODULE- II

Gate triggering circuits – R, RC, UJT triggering circuits – natural and forced commutation (concept only). Requirements of isolation and synchronization in gate drive circuits- Opto and pulse transformer based isolation.

Controlled rectifiers – half-wave controlled rectifier with R load – 1-phase fully controlled bridge rectifier with R, RL and RLE loads (continuous & discontinuous conduction) – output voltage equation – 1- phase half controlled bridge rectifier with R, RL and RLE loads – displacement power factor – distortion factor.

Gate triggering circuits

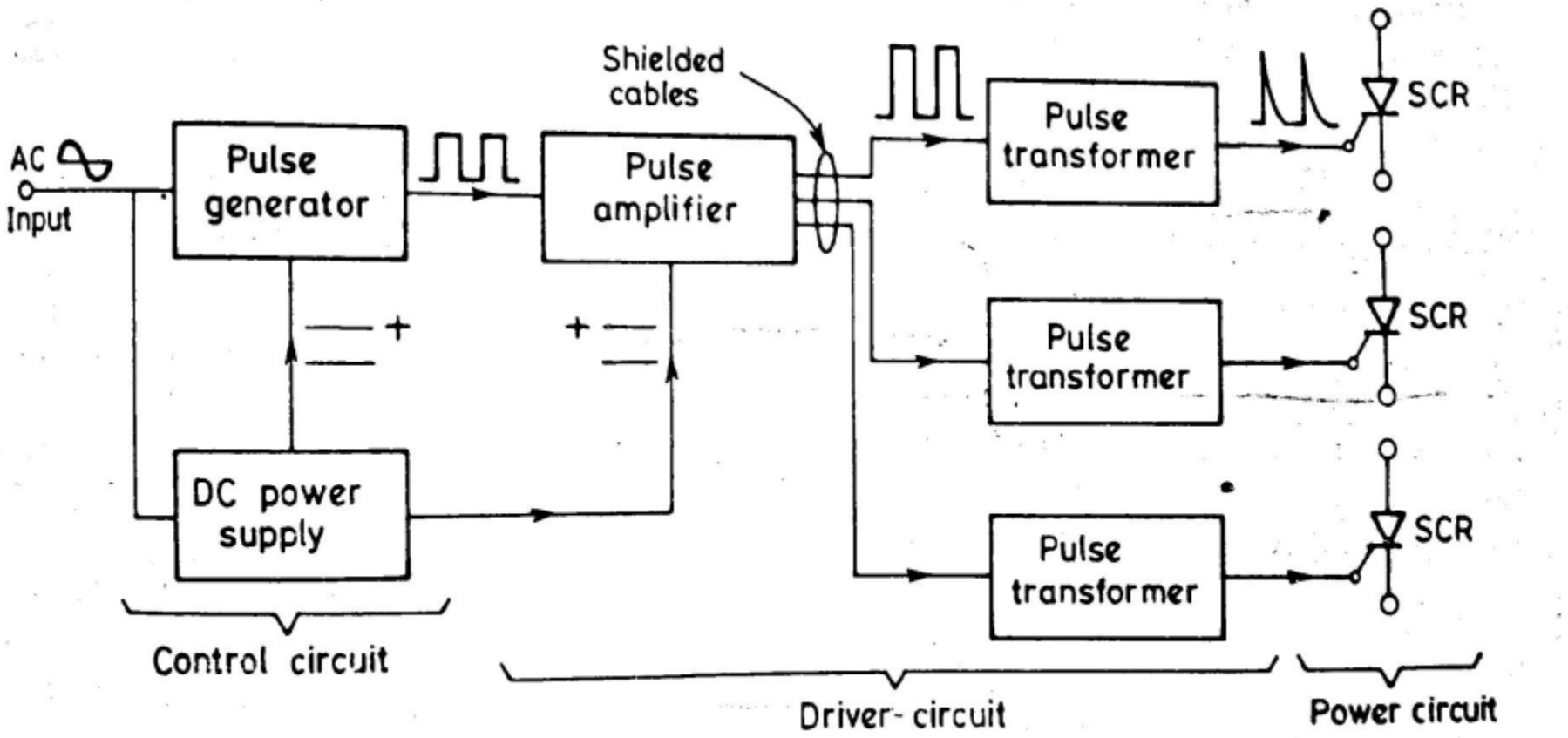
- An SCR can be switched from off-state to on-state in several ways

1. Forward voltage triggering
2. dv/dt triggering
3. Temperature triggering
4. Light triggering
5. Gate triggering

- The instant of turning on the SCR cannot be controlled by first three methods
- Light triggering used in some applications especially in series connected string
- Gate triggering – most common method, efficient and reliable

Main features of firing circuits

- Gate control circuit is also called firing or triggering circuit
- Gate circuits are usually low power electronics circuits

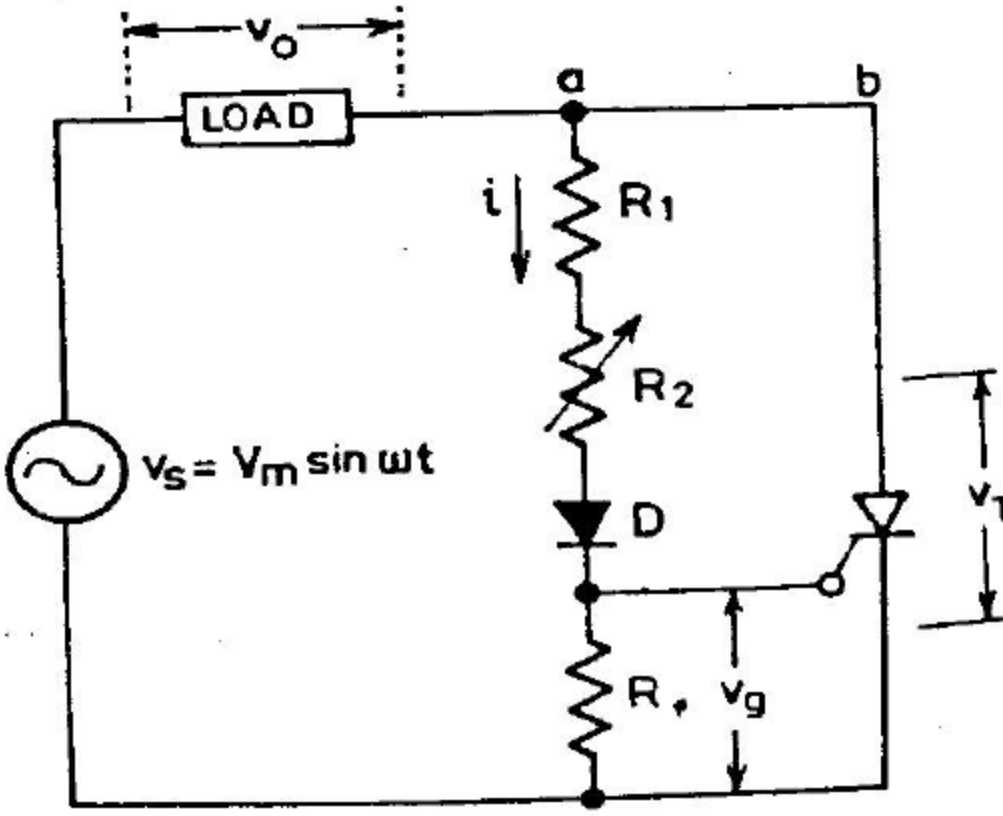


Main features of firing circuits

- A firing circuit should fulfill the following two functions
- If power circuit has more than one SCR, the firing circuit should produce gating pulses for each SCR at the desired instant for proper operation of the power circuit
- The control signal generated by a firing circuit may not be able to turn on an SCR. It is therefore common to feed the voltage pulse to a driver circuit and then to a gate cathode circuit

R triggering circuit (Resistance triggering)

- Simplest and most economical
- Suffer from a limited range of firing angle control (0 to 90°)
- R2 - variable resistance
- R – stabilizing resistance
- In case R2=0, gate current may flow from source, trough load, R1, D and gate to cathode



R triggering circuit (Resistance triggering)

- This current should not exceed maximum permissible gate current Igm
- R1 therefore found from the relation

$$\frac{V_m}{R_1} \leq I_{gm} \qquad or\ R_1 \geq \frac{V_m}{I_{gm}}$$

- Function of R1 is to limit the gate current to a safe value as R2 is varied
- Resistance R should have a value such that maximum voltage drop across it does not exceed maximum possible gate voltage Vgm

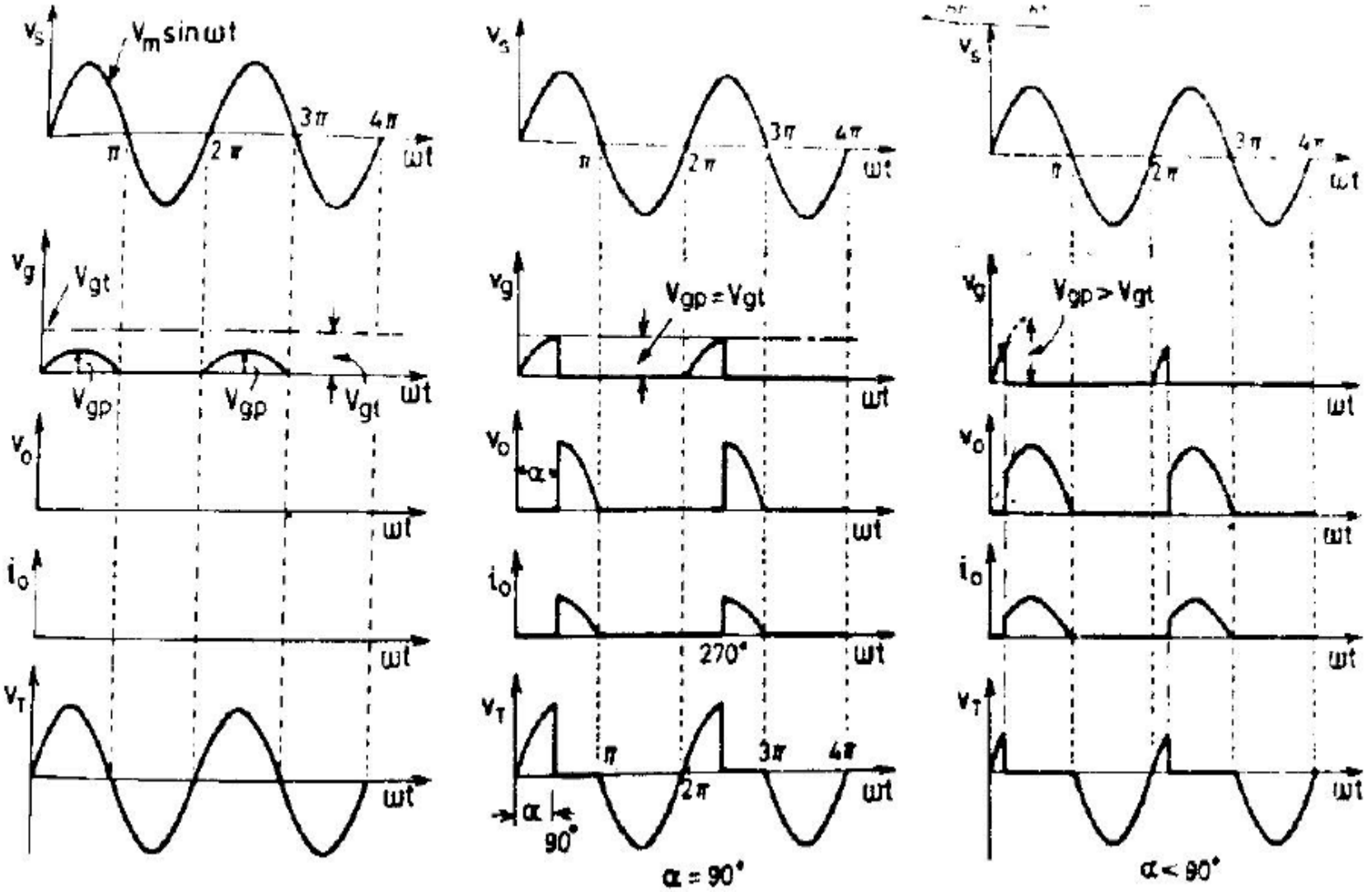
- This can happen only when R2 is zero
- Under this condition

$$\frac{V_m}{R_1 + R} . R \leq V_{gm}$$

- As resistance R1, R2 are large, gate trigger circuit draws a small current
- Diode D allows the flow of current during positive half cycle only
- The amplitude of this dc pulse can be controlled by varying R2

- The potentiometer setting R2 determines the gate voltage amplitude
- When R2 is large current i is small and the voltage across R,vg=i.R is also small
- As Vgp is less than Vgt, SCR will not turn on
- Therefore load voltage vo=0, io=0 and supply voltage appear across SCR
- Trigger circuit consist of resistance only, therefore vg is in phase with source voltage vs
- R2 is adjusted such that Vgp=Vgt, this gives the value of firing angle as 90

R triggering circuit (Resistance triggering)



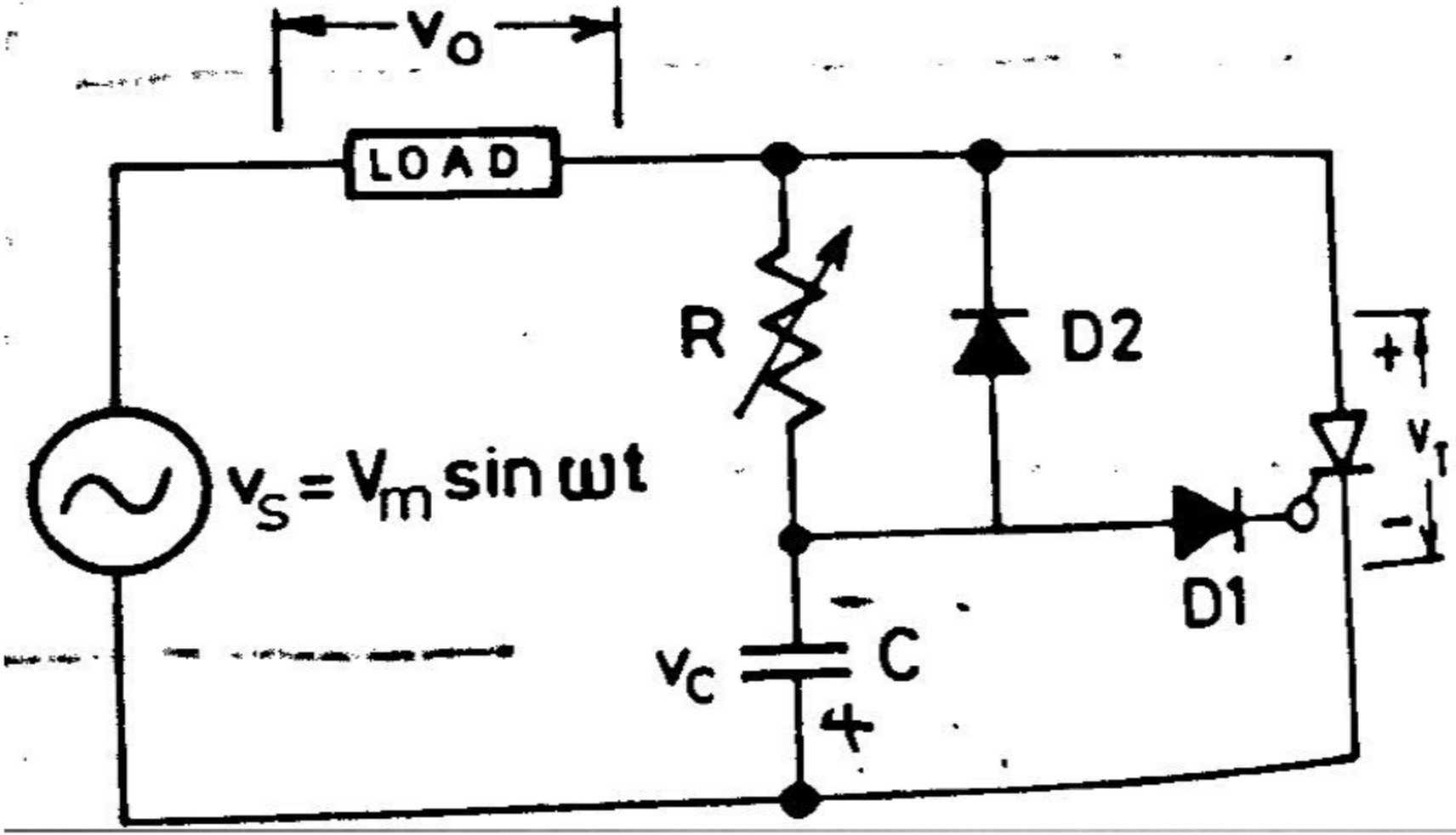
- The same circuit also is applicable for TRIAC.
- However, diode D1 has to be removed such that a trigger signal will be available at the gate terminal during both half-cycles.
- Because the gate of a TRIAC is not equally sensitive in all four of its modes of switching, α and hence vo are usually different in the positive and negative half-cycles of the supply voltage.

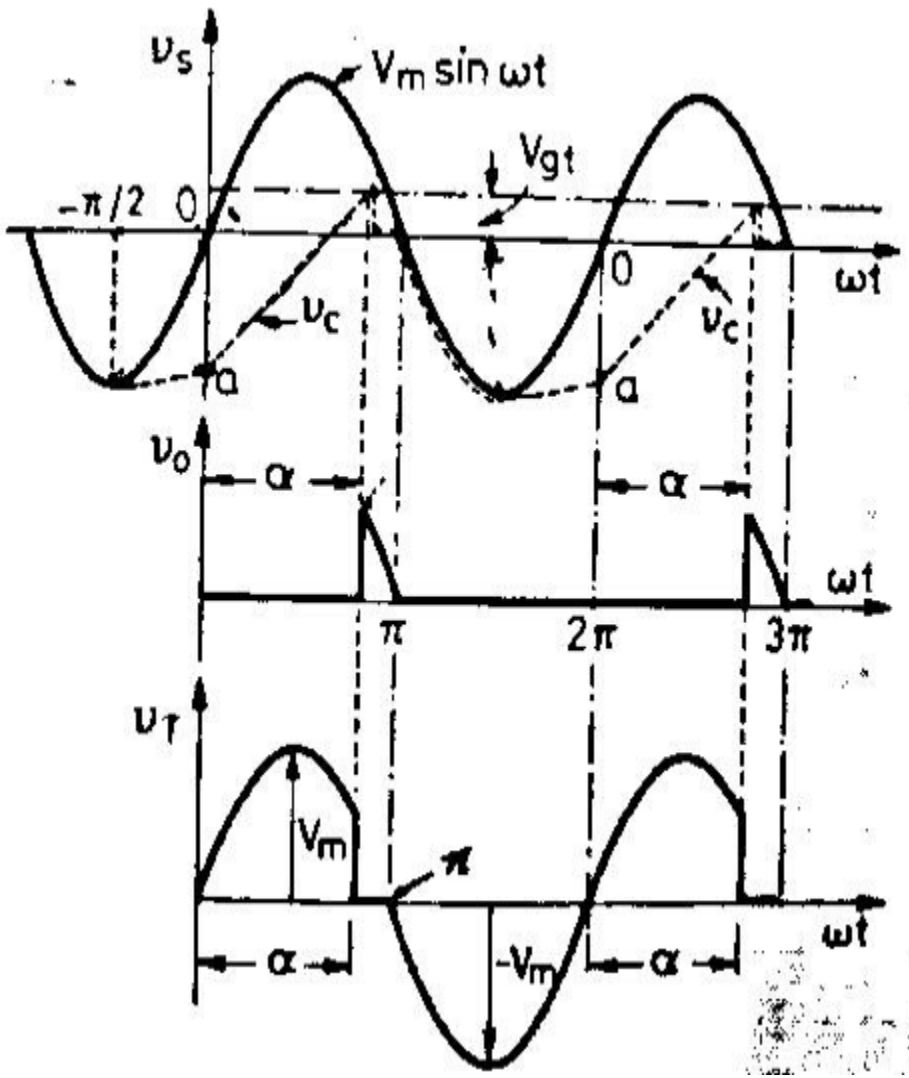
RC triggering circuit

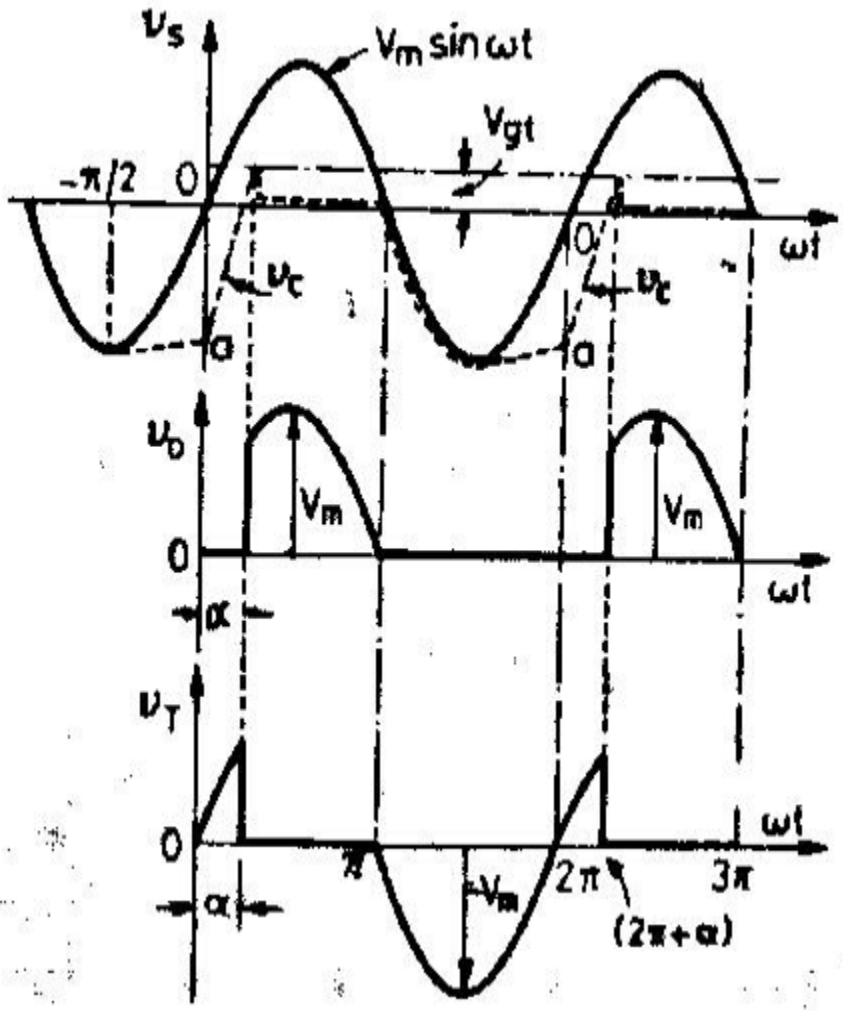
- The limited range of firing angle control by resistance firing circuit can be overcome by RC firing circuit
- Several variations of RC trigger circuits are available
- In these cases the range of α is extendable beyond 90.

RC half wave triggering circuit

- By varying the value R, firing angle can be controlled from 0 to 180
- In the –ve half cycle capacitor C charges through D2 with lower plate +ve to the peak supply voltage Vm at $\omega t=-90$
- After $\omega t=-90$, source voltage Vs decreasing from –Vm at $\omega t=-90$ to zero at $\omega t=0$


v_o
LOAD
R
D2
+
v_T
-
$v_s = V_m \sin \omega t$
D1
v_C
C
+


v_s
$V_m \sin \omega t$
V_{gt}
$-\pi/2$
0
ωt
v_c
a
v_o
α
π
2π
3π
v_T
V_m
$-V_m$


v_s
$V_m \sin \omega t$
V_{gt}
$-\pi/2$
0
ωt
v_c
a
v_o
V_m
α
v_T
$-V_m$
2π
3π
$(2\pi+\alpha)$

- During this period capacitor voltage may fall from -Vm to some small value -oa
- Now the charging of the capacitor (with upper plate positive) takes place through R and the charging rate depends on the time-period RC.
- When capacitor charges to +ve voltage equal to VGT , conduction of the SCR takes place.
- After this capacitor holds a small +ve voltage
- Diode D1 used to prevent the breakdown of cathode to gate junction through D2 during the –ve cycle

- where the angular frequency of ac mains $\omega t = 2\pi/T$.

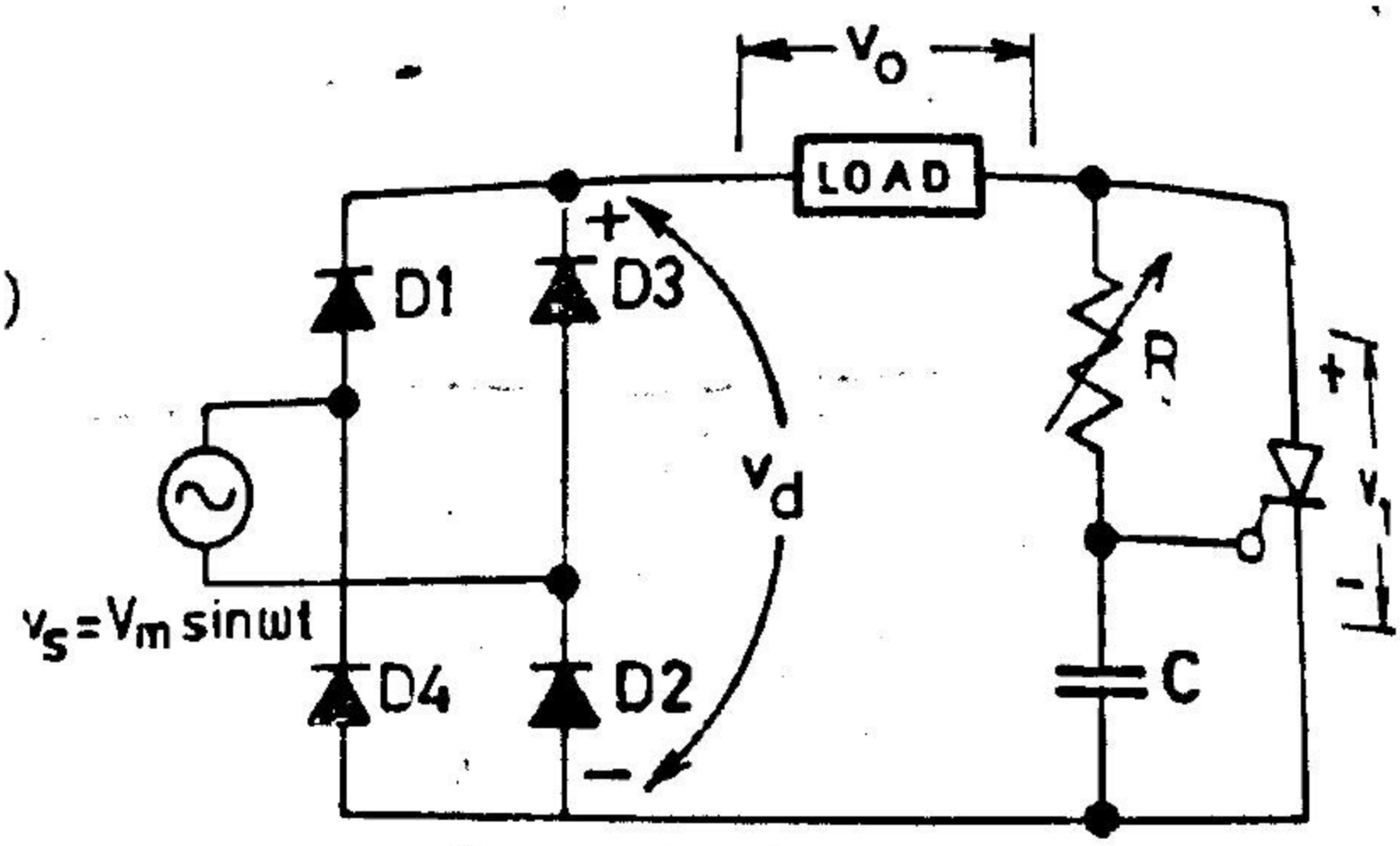
$$RC \geq \frac{1.3\,T}{2} = \frac{4}{\omega}$$

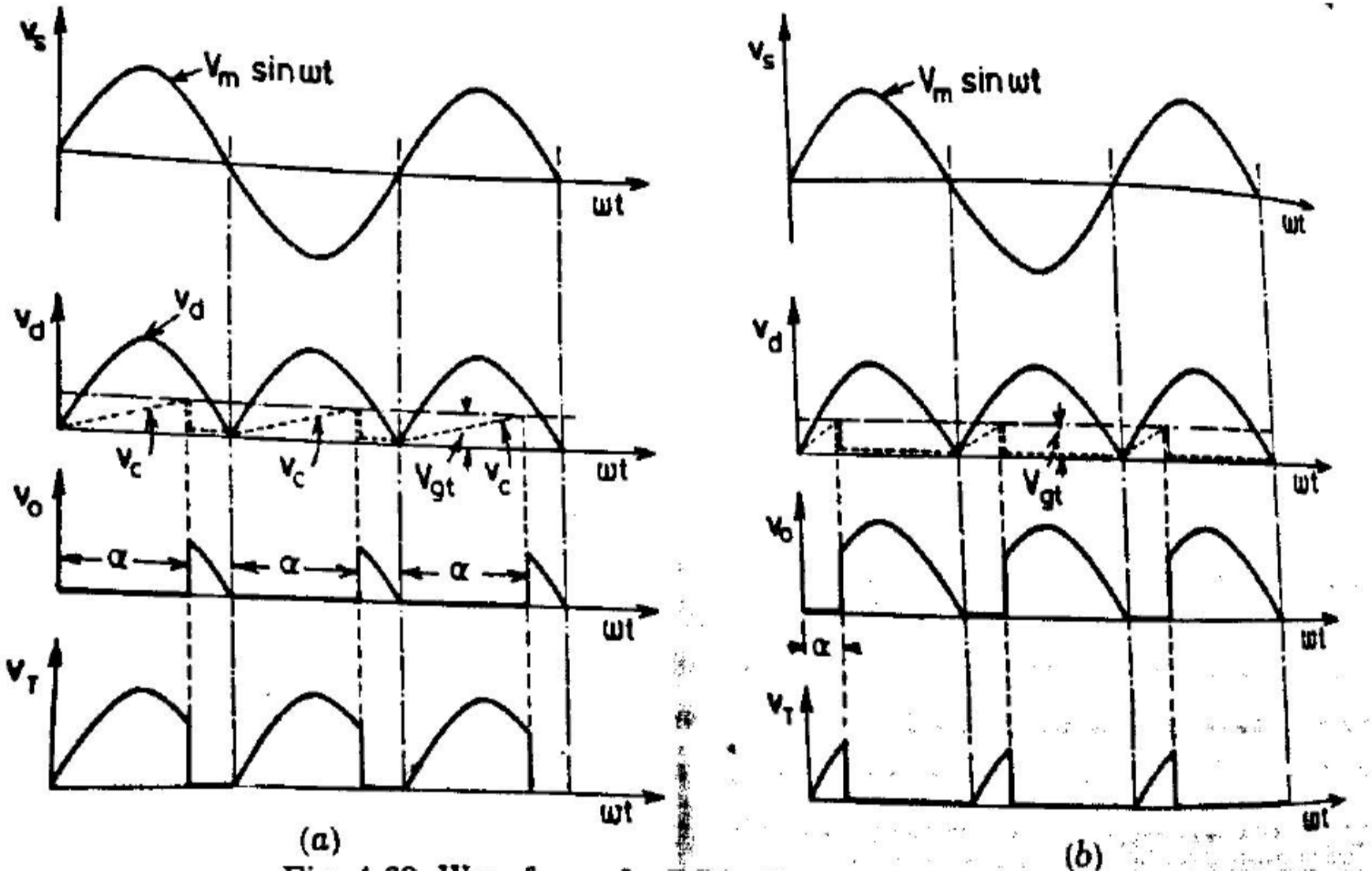
- The value of R is chosen such that the required I_{GT} and V_{GT} are supplied to the gate terminal:

$$R \leq \frac{V_s - V_{gt} - v_d}{I_{gt}}$$

- Where v is the voltage at the switching instant of thyristor and v_D is forward voltage drop of diode D1

RC Full wave triggering circuit




v_s
$V_m \sin \omega t$
ωt
v_d
v_d
v_c
v_c
V_{gt}
v_c
ωt
v_o
α
α
α
ωt
v_T
ωt
(a)
v_s
$V_m \sin \omega t$
ωt
v_d
V_{gt}
ωt
v_o
α
ωt
v_T
ωt
(b)

- Diode D1-D4 form a full – wave diode bridge
- When capacitor charges to a voltage equal to Vgt, SCR triggers and rectified voltage Vd appears across load as Vo
- The value of RC can be calculated by

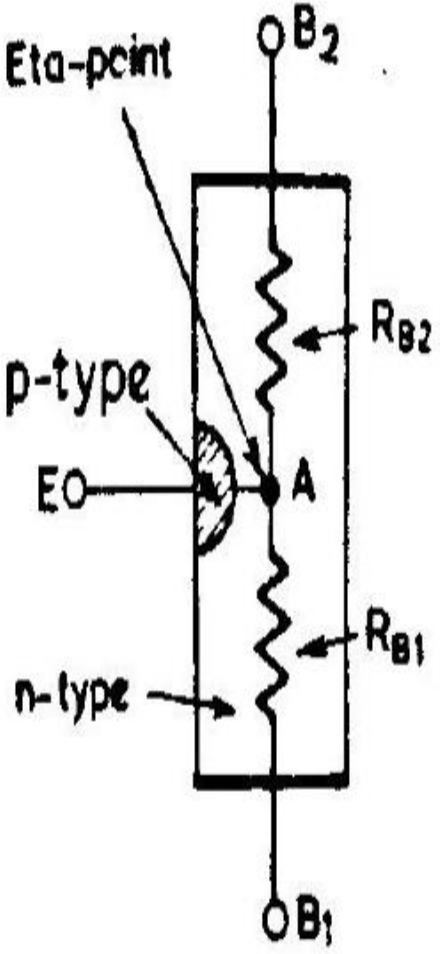
$$RC \geq 50.\frac{T}{2} = \frac{157}{\omega}$$

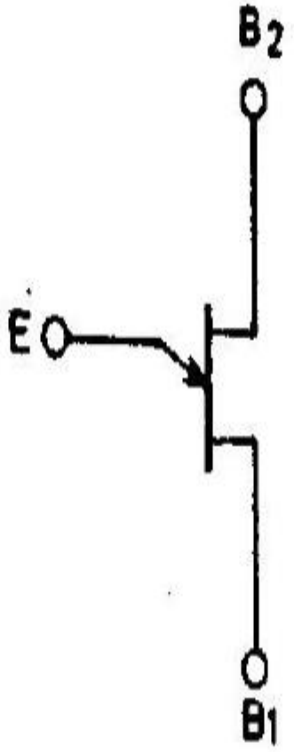
- R is given by

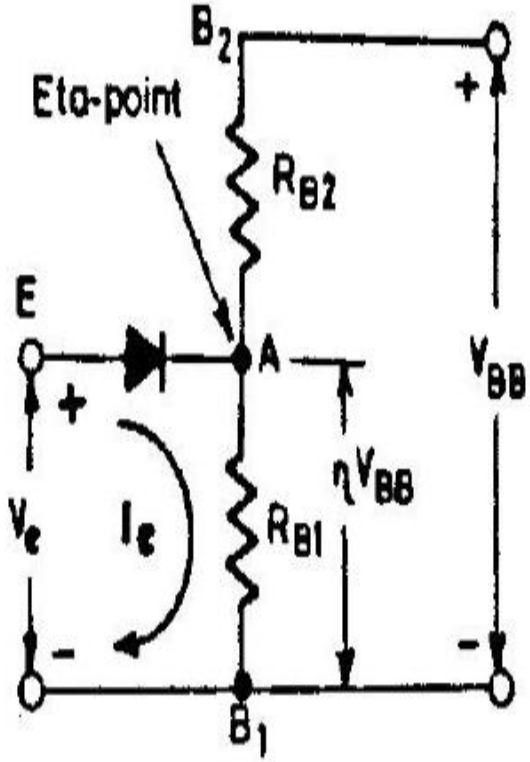
$$R \ll \frac{V_s - V_{gt}}{I_{gt}}$$

UJT triggering circuit

- Resistance and RC triggering circuits described above gives prolonged pulses
- As a result power dissipation in the gate circuit is large
- At the same time, R and RC triggering circuits cannot be used for automatic or feedback control system
- These difficulties can be overcome by use of UJT triggering circuits
- An UJT is made up of an n-type silicon base to which p-type emitter is embedded
- The n-type base is slightly doped whereas p-type is heavily doped


Eta-point
B2
RB2
p-type
E
A
RB1
n-type
B1


B2
E
B1


B2
Eta-point
RB2
E
A
+
VBB
+
ηVBB
Ve
Ie
RB1
-
-
B1

- The two ohmic contacts provided at each end are called base-one B1 and base-two B2
- So an UJT is a three terminal device emitter, base one and base two
- The emitter terminal divides the inter base resistance (VBB) into two parts (say, RB1 and RB2).
- If a dc biasing voltage (VBB) is applied across the base terminals, the voltage in N-type material near emitter terminal (k) is given by

$$V\eta = \frac{R_{B1}}{R_{B1} + R_{B2}} = \eta V_{BB}$$

- where η is called the intrinsic-standoff ratio of UJT and its value is less than unity (typical value varies between 0.5 and 0.85).

- The UJT is highly efficient switch; its switching time is in the range of nanoseconds
- Since UJT exhibit negative resistance characteristics, it can be used as a relaxation oscillator

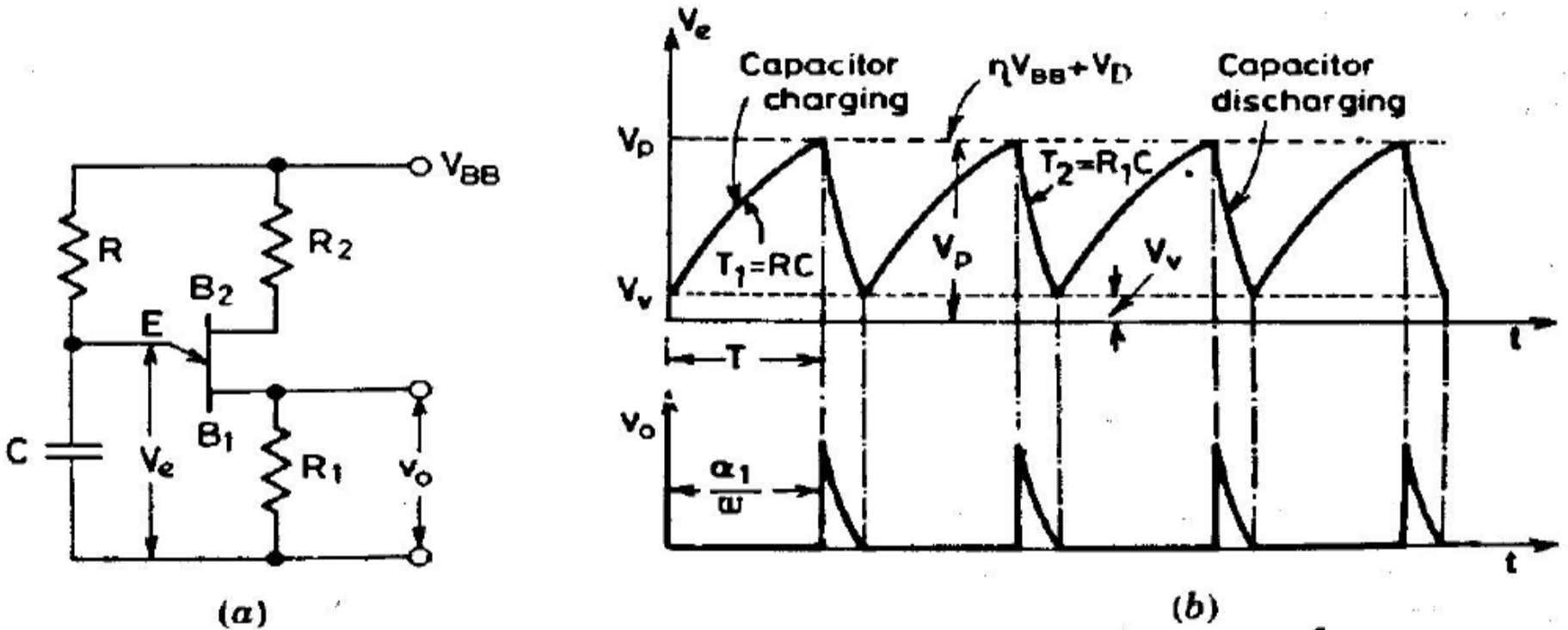


Fig. 4.72. UJT oscillator (*a*) Connection diagram and (*b*) Voltage waveforms.

- The external resistance R1 and R2 are small in comparison with the internal resistances RB1 and RB2
- The charging resistance R should be such that its load line intersect the device characteristics only in the –ve resistance region
- When source voltage VBB is applied, capacitor C begins to charge through R exponentially towards VBB
- The time constant of the charge circuit is

$$\tau_1 = RC$$

- When this emitter voltage reaches peak-point voltage Vp, the uni-junction between E-B1 breaks down

- As a result, UJT turns on and capacitor C rapidly discharges through low resistance R1 with a time constant

$$\tau_2 = R_1 C$$

- When emitter voltage decays to the valley-point voltage Vv, emitter current falls below Iv and UJT turns off
- The time T required for the capacitor C to charge from initial voltage Vv to peak-point voltage Vp through large resistance R can be obtained as

$$V_p = \eta V_{BB} + V_D = V_v + V_{BB}\left(1 - e^{-T/RC}\right)$$

$$V_D = V_v, \eta = (1 - e^{-T/RC})$$

$$T = \frac{1}{f} = RC \ln\left(\frac{1}{1-\eta}\right)$$

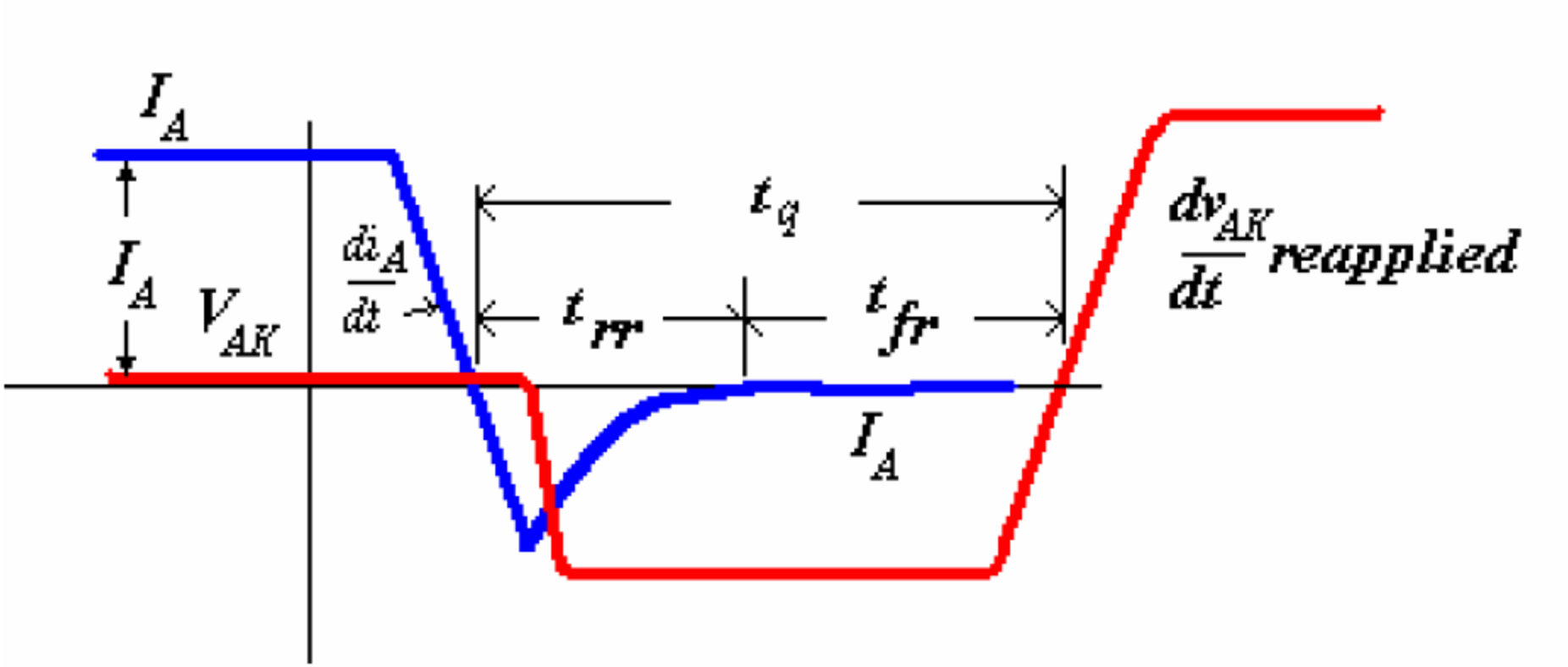
- The charging of the capacitor starts from each zero crossover instant only.
- The first pulse in each half-cycle that triggers the thyristor is synchronized with v, and therefore α becomes equal in each cycle.
- By controlling R, the time period of oscillator (τ), or the delay period of the first pulse (τ), α can be adjusted.
- The UJT trigger circuit may also be energized from a separate transformer (for biasing) and the same performance can be achieved.

Natural and forced commutation

- A thyristor can be turned ON by applying a positive voltage of about a volt or a current of a few tens of milliamps at the gate-cathode terminals.
- However, the amplifying gain of this regenerative device being in the order of the 10^8, the SCR cannot be turned OFF via the gate terminal.
- It will turn-off only after the anode current is annulled either naturally or using forced commutation techniques.
- These methods of turn-off do not refer to those cases where the anode current is gradually reduced below Holding Current level manually or through a slow process.
- Once the SCR is turned ON, it remains ON even after removal of the gate signal, as long as a minimum current, the Holding Current, Ih, is maintained in the main or rectifier circuit.

Natural and forced commutation

Turn off dynamics of SCR



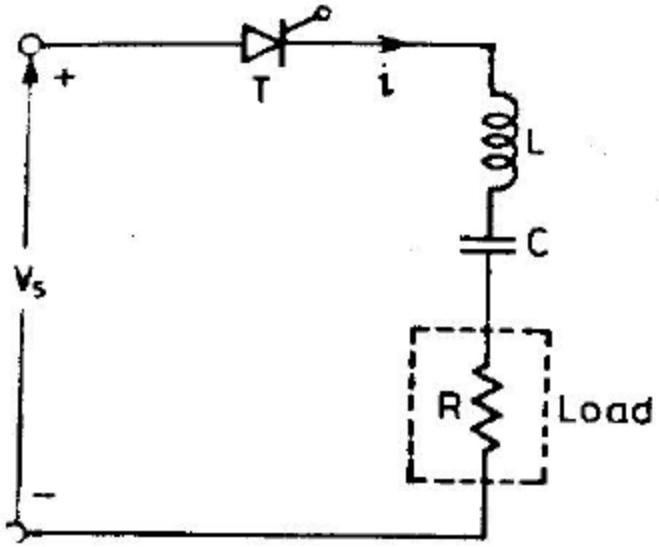
- In all practical cases, a negative current flows through the device.
- This current returns to zero only after the reverse recovery time trr, when the SCR is said to have regained its reverse blocking capability.
- The device can block a forward voltage only after a further tfr, the forward recovery time has elapsed.
- Consequently, the SCR must continue to be reverse-biased for a minimum of tfr + trr = tq, the rated turn-off time of the device.
- The external circuit must therefore reverse bias the SCR for a time toff > tq. Subsequently, the reapplied forward biasing voltage must rise at a dv/dt < dv/dt (reapplied) rated.

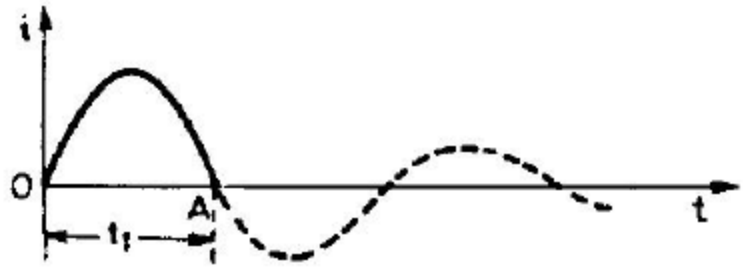
- SCRs have turn-off times rated between 8 - 50 μsecs.
- The faster ones are popularly known as 'Inverter grade' and the slower ones as 'Converter grade' SCRs.
- The latter are available at higher current levels while the faster ones are expectedly costlier

The six distinct classes by which the SCR can be turned off are:

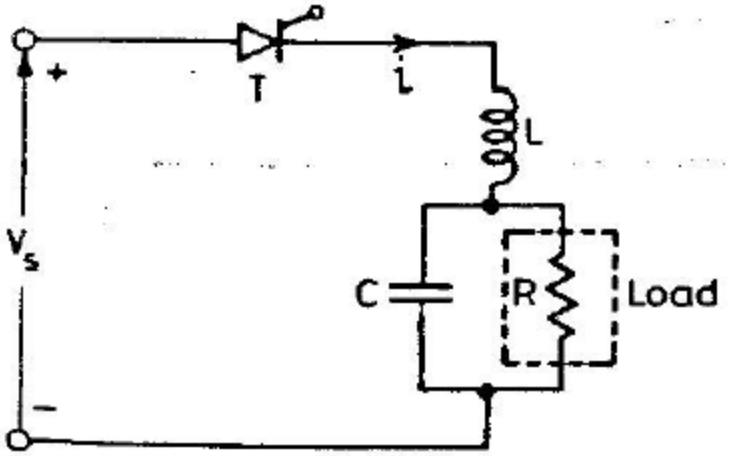
- Class A Self commutated by a resonating load
- Class B Self commutated by an L-C circuit
- Class C C or L-C switched by another load carrying SCR
- Class D C or L-C switched by an auxiliary SCR
- Class E An external pulse source for commutation
- Class F AC line commutation

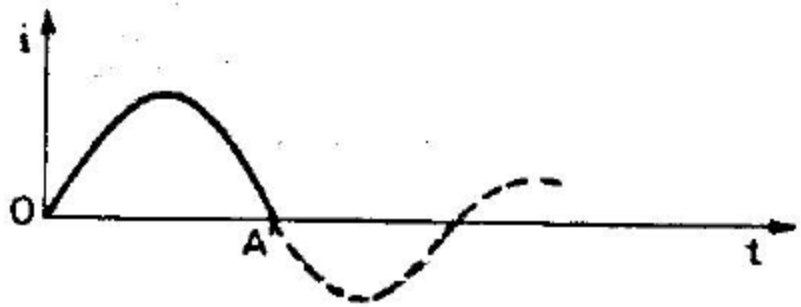
Class A Commutation: Load commutation





(a)

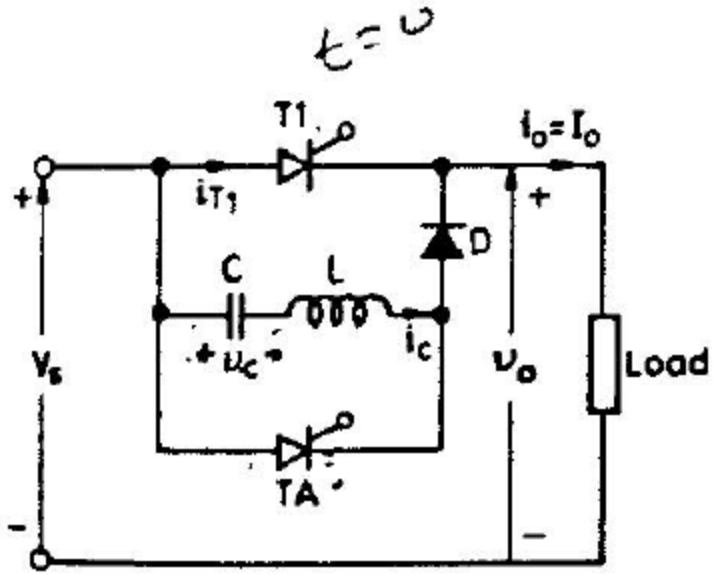




(b)

- R is load resistance
- For low values of R, - R, L and C can be connected in series
- For high values of R – L and R are connected in parallel
- Essential requirement for both the circuit – overall circuit must be under-damped
- When energized from dc source, current builds up like sinusoidal wave form
- Current first rises to maximum value and then decreases
- When current decays to zero and tends to reverse, SCR T is turned off
- Possible only in dc circuit
- Also called - resonant commutation, self commutation or load commutation

Class B: Resonant pulse commutation

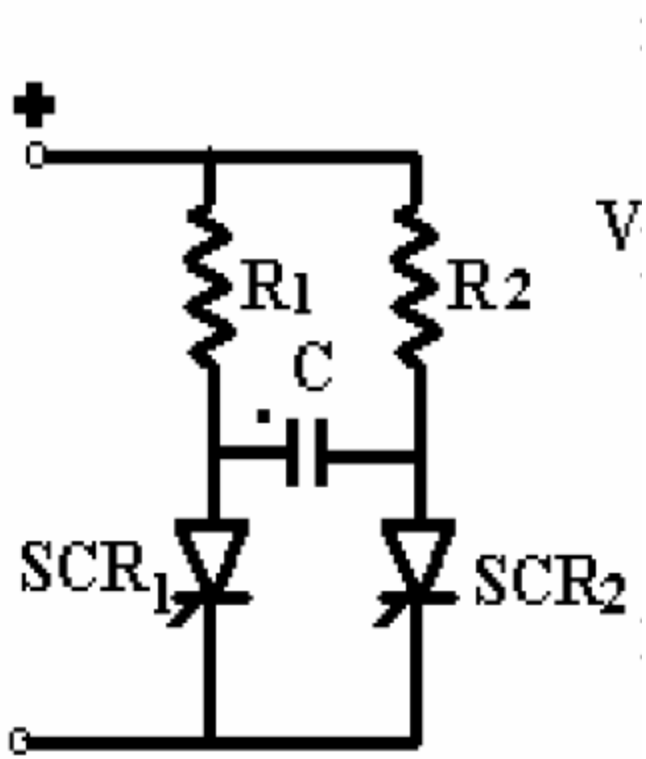


- Source voltage Vs charges capacitor C to voltage Vs with left hand plate +ve
- Main thyristor as well as auxiliary thyristor are off
- When T1 is turned on at t=0, constant current Io is is established in the load circuit
- Up till time t1; ic=0, vc=Vs,io=Io iT1=Io
- For initiating the commutation of main thyristor T1, auxiliary thyristor TA is gated at t=t1
- With TA on, a resonant current ic begins to flow from C through TA, L and back to C

$$i_c = -V_s\sqrt{\frac{C}{L}}\sin\omega_0 t$$

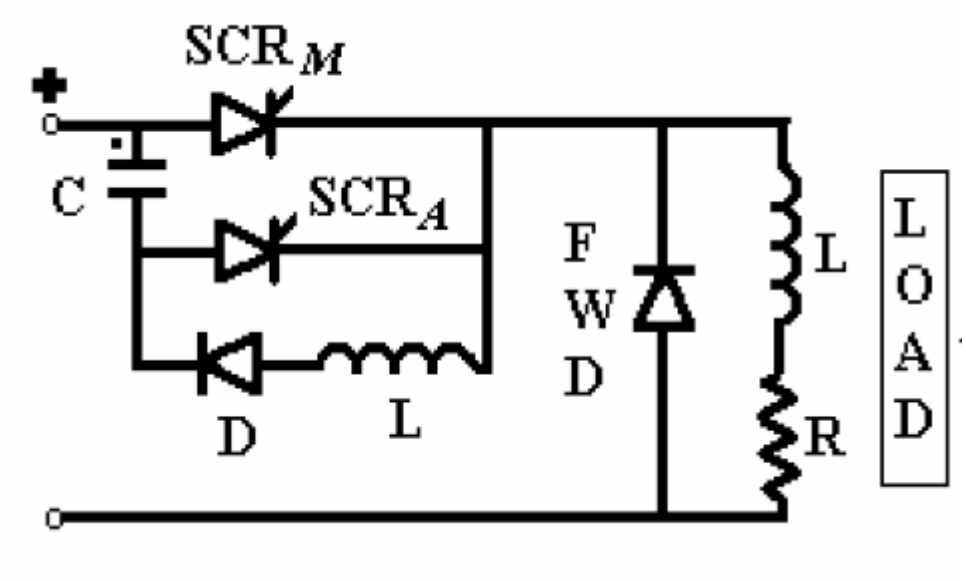
- -ve sign is due to the fact that, this current flows opposite to the reference +ve direction chosen for ic
- At t1; ic=0, vc=-Vs and iT1=Io
- Just after t2, ic tends to reverse , TA is turned off at t2
- With vc=-Vs, right hand plate has +ve polarity
- Resonant current ic now builds up through C, L, D and T1
- As this current ic grows opposite to forward thyristor current of T1, net forward current iT1=Io-ic begins to decrease
- Finally when ic in the reversed direction attains the value Io, forward current in T1 is reduced to zero and the device T1 is turned off at t3

Class C, C or L-C switched by another load–carrying SCR



- This configuration has two SCRs.
- One of them may be the main SCR and the other auxiliary.
- Both may be load current carrying main SCRs.
- The configuration may have four SCRs with the load across the capacitor, with the integral converter supplied from a current source.
- Assume SCR^2 is conducting. C then charges up in the polarity shown.
- When SCR^1 is triggered, C is switched across SCR^2 via SCR^1 and the discharge current of C opposes the flow of load current in SCR^2.

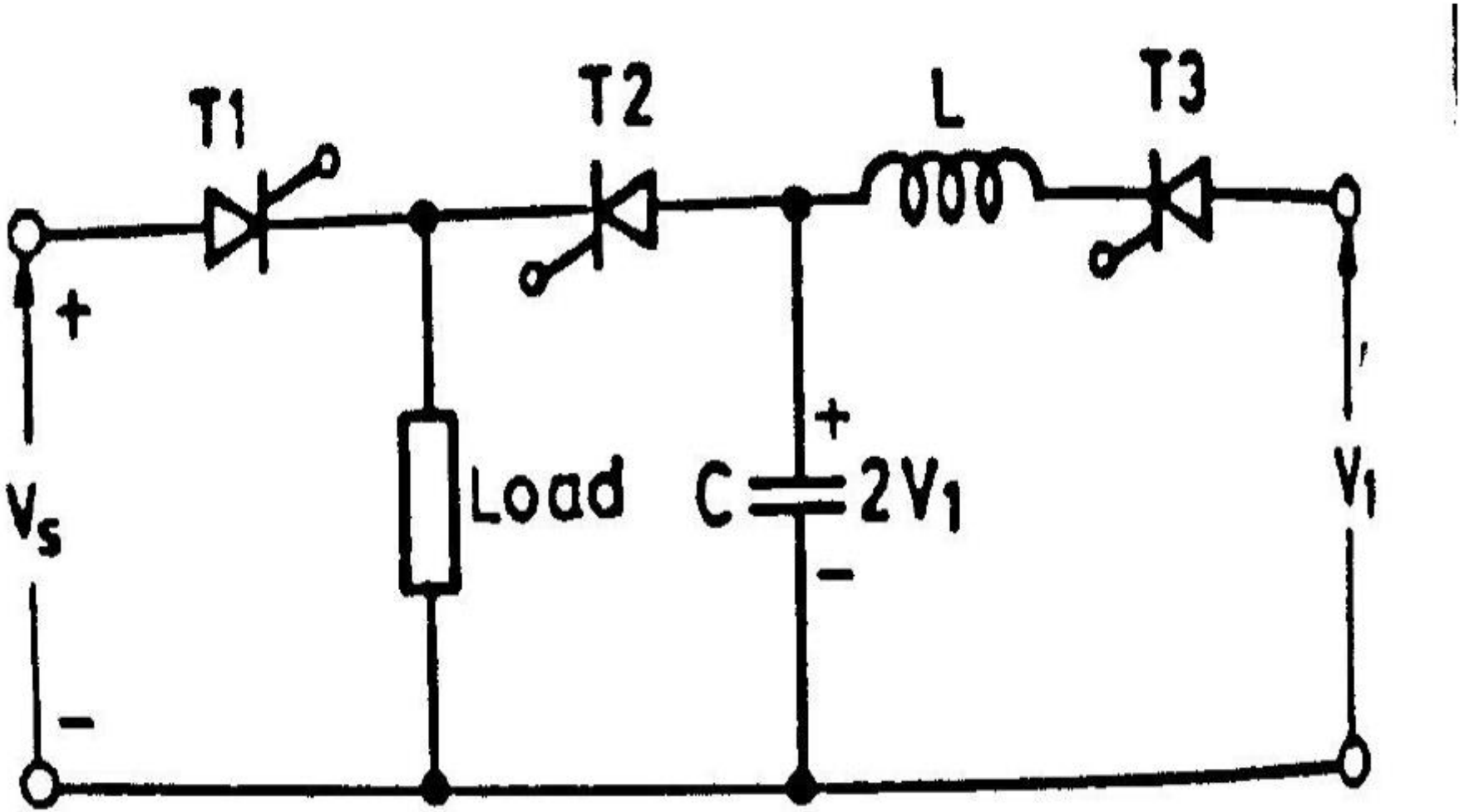
Class D, L-C or C switched by an auxiliary SCR



- Class C can be converted to Class D if the load current is carried by only one of the SCR's, the other acting as an auxiliary turn-off SCR.
- The auxiliary SCR would have a resistor in its anode lead of say ten times the load resistance.
- SCRA must be triggered first in order to charge the upper terminal of the capacitor as positive.
- As soon as C is charged to the supply voltage, SCRA will turn off.

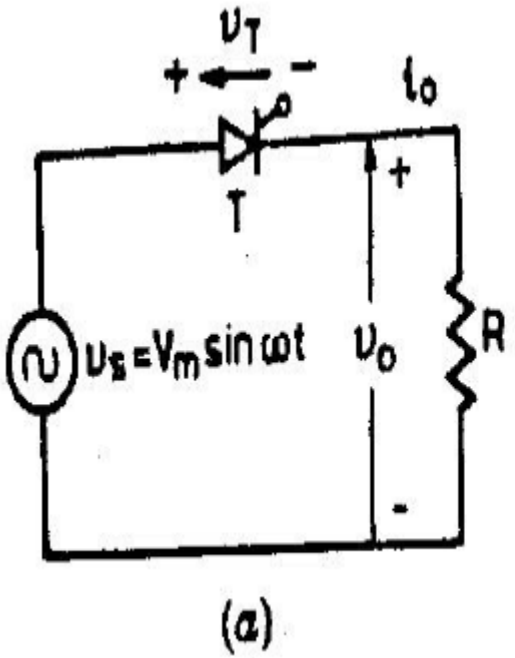
- If there is substantial inductance in the input lines, the capacitor may charge to voltages in excess of the supply voltage.
- This extra voltage would discharge through the diode-inductor-load circuit.
- When SCRM is triggered the current flows in two paths: Load current flows through the load and the commutating current flows through C- SCRM -L-D network.
- The charge on C is reversed and held at that level by the diode D.
- When SCRA is re-triggered, the voltage across C appears across SCRM via SCRA and SCRM is turned off.

Class E – External pulse commutation

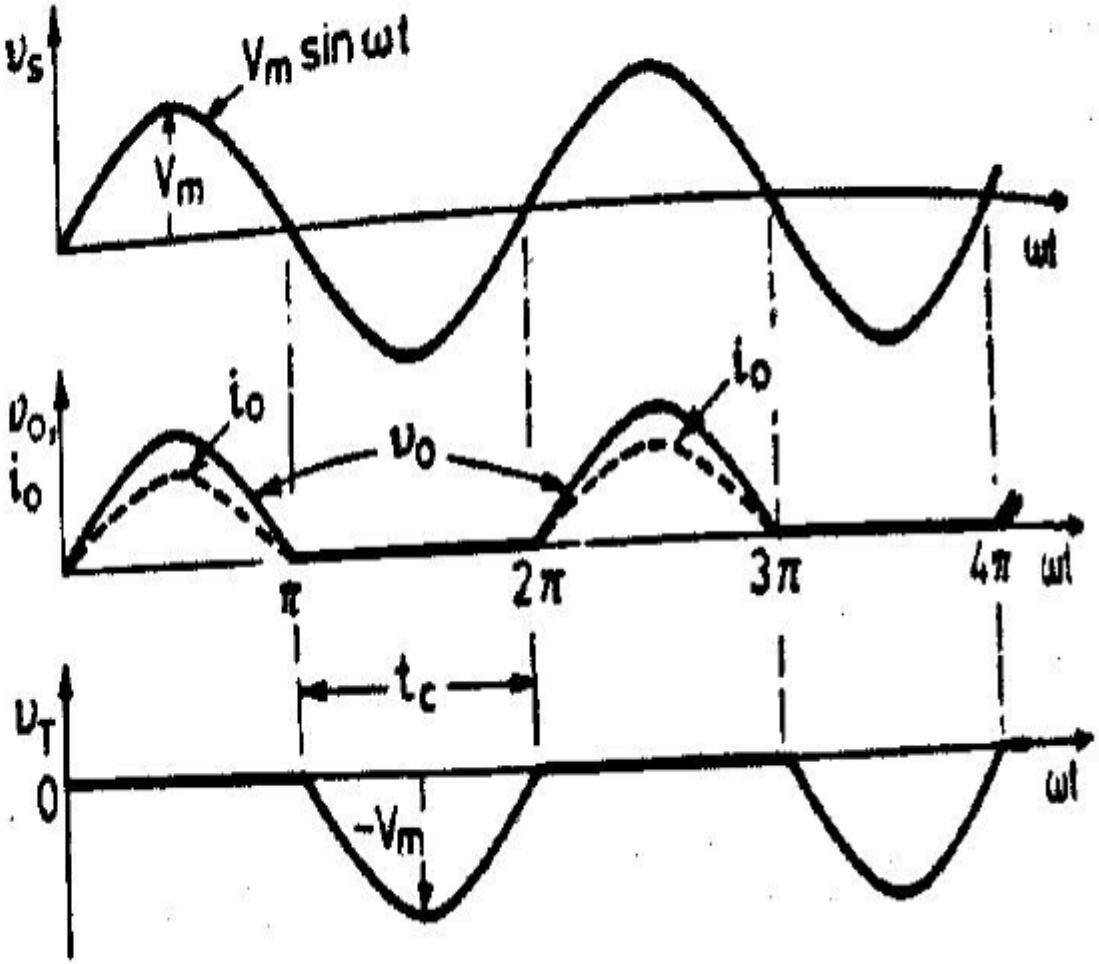


- A pulse of current is obtained from a separate voltage source to turn off the conducting SCR
- The peak value of the current pulse must be more than the load current
- Vs is the voltage of main source and V1 is the voltage of auxiliary supply
- Thyristor T1 is conducting and load is connected to Vs
- When T3 is turned on, V1, T3, L and C form an auxiliary circuit
- Therefore C is charged to a voltage +2V1and auxiliary current falls to zero T3 gets commutated
- For turning off T1, T2 is turned on
- With T2 on, T1 is subjected to a reverse voltage, Vs-2V1 and T1 is therefore turned off
- After T1 turned off, capacitor discharges through load

Class F : Line commutation



(a)

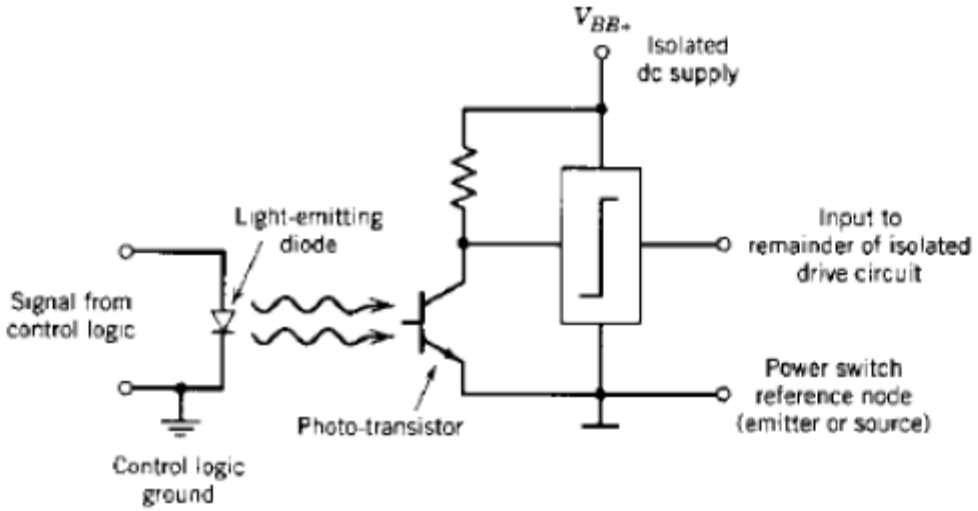


(b)

- Can occur only when source is ac
- When SCR is energized from ac source, current has to pass through its natural zero at the end of every +ve half cycle
- Then ac source apply a reverse voltage across SCR automatically
- As a result SCR turned off
- This is called natural commutation, because no external circuit is employed to turn off the thyristor

Optocouplers

- Consist of a light emitting diode (LED), the output transistor and a built in schmitt trigger
- A +ve signal from the control logic causes the LED to emit light that is focused on the optically sensitive base region of a photo transistor

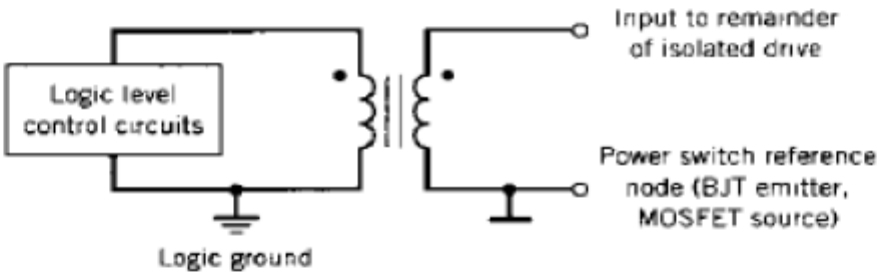


- The light falling on the base region generate a significant number of electron hole pair in the base region that causes the photo transistor to turn on
- The resulting drop in voltage at the photo transistor collector causes the schmitt trigger to change state
- The output of the schmitt trigger is the optocoupler output and can be used as the control input to the isolated drive circuit
- The capacitance between LED and the base of the receiving transistor within the optocoupler should be as small as possible to avoid retriggering at both turn on and turn off of the power transistor due to the jump in the potential between the power transistor emitter reference point and the ground of the control electronics

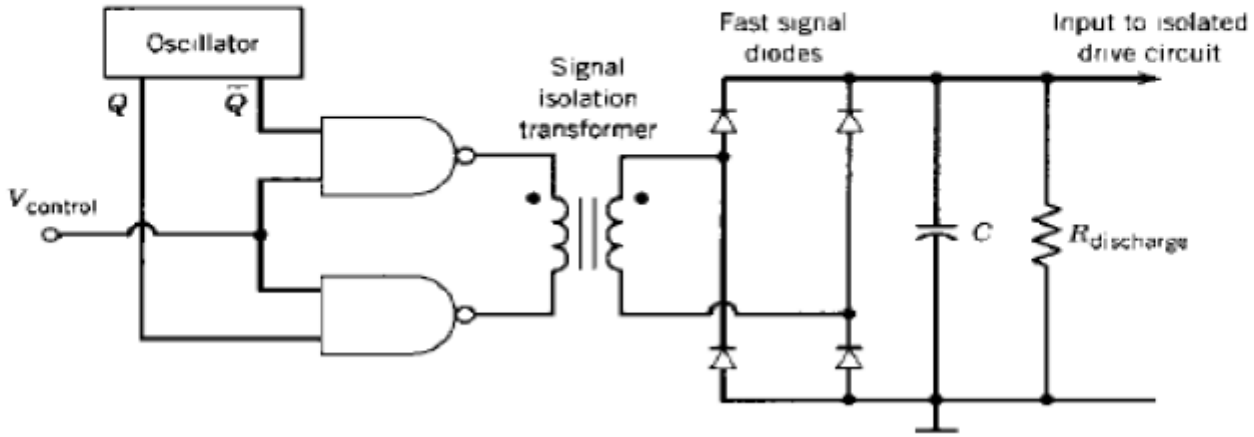
- To reduce this problem optocouplers with electrical shield between the LED and the receiver transistor should be used
- As an alternative, fiber optic cables can be used to completely eliminate this retriggering problem and to provide very high electrical isolation and creepage distance
- When using fiber optic cables, the LED is kept on the printed circuit board of the control electronics, and the optical fiber transmits the signal to the receiver transistor which is put on the drive circuit printed circuit board

Pulse transformer

- Instead of using optocouplers or fiber optic cables, the control signal can be coupled to the electrically isolated drive circuit by means of a transformer



(a)



(b)

- If the switching frequency is high and the duty ratio D varies only slightly around 0.5, a baseband control signal of appropriate magnitude can be applied directly to the primary of a relatively small and light weight pulse transformer as in (a)
- And the secondary output can be used to either directly drive the power switch or used as the input to an isolated drive circuit
- As the switching frequency is decreased below the tens of kilohertz range, a baseband control signal directly applied to the transformer primary becomes impractical because the size and weight of the transformer becomes increasingly larger

- Modulation of a high frequency carrier by a low frequency control signal enables a small high frequency pulse transformer to be used for even low frequency control signal
- In fig.b. the control signal modulates a high frequency oscillator output before being applied to the primary of a high frequency signal transformer
- Since a high frequency transformer can be made quite small, it is easy to avoid stray capacitance between the input and output winding and the transformer will be inexpensive
- The transformer secondary output is rectified and filtered and then applied to the comparator and the rest of the isolated drive circuit

Controlled rectifiers – Principles of phase control

- the firing angle may defined as the angle between the instant thyristor would conduct if it were a diode and the instant it is triggered
- Is measured form the angle that gives the largest average output voltage or the highest load voltage
- It is also defined as the angle measured from the instant that gives the largest output voltage to the instant it is triggered
- Angle measured from the instant SCR gets forward biased to the instant it is triggered

Single phase half controlled

- Single phase half controlled rectifier with R load
- Single phase half controlled rectifier with R L load
- Single phase half controlled rectifier with R L load and freewheeling diode
- Single phase half controlled rectifier with R L E load
- Single phase half controlled rectifier with R L E load and freewheeling diode

Single phase full controlled

- Single phase full controlled rectifier with R load
- Single phase full controlled rectifier with R L load (Continues conduction)
- Single phase full controlled rectifier with R L load (Discontinues conduction)
- Single phase full controlled rectifier with R L load and freewheeling diode
- Single phase full controlled rectifier with R L E load (Continues conduction)
- Single phase full controlled rectifier with R L E load (Discontinues conduction)
- Single phase full controlled rectifier with R L E load and freewheeling diode

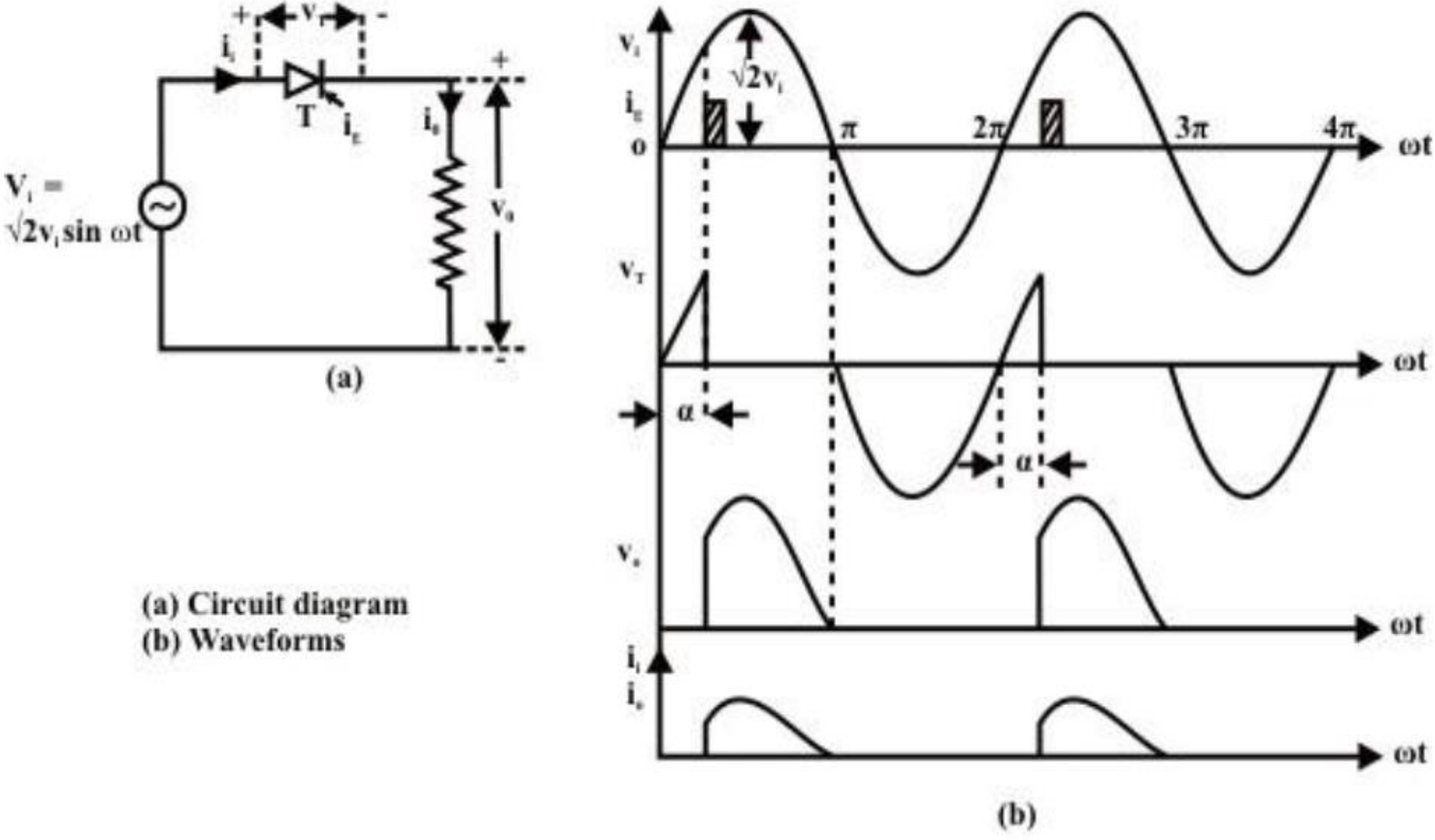
Single phase semi converter

- Single phase semi-converter with R load
- Single phase semi-converter with R L load (Continues conduction)
- Single phase semi-converter with R L load (Discontinues conduction)
- Single phase semi-converter with R L load and freewheeling diode
- Single phase semi-converter with R L E load (Continues conduction)
- Single phase semi-converter with R L E load (Discontinues conduction)
- Single phase semi-converter with R L E load and freewheeling diode

Single phase half wave circuit with R load

- The source voltage is $v_s = V_m \sin \omega t$
- An SCR can conduct only when anode voltage is +ve and a gate signal is applied
- At some delay angle α, a +ve gate signal applied between gate and cathode turns on the SCR
- Immediately full supply voltage is applied across the load
- At the instant of angle α, Vo rises from zero to $V_m \sin \omega t$
- Thyristor remains on from $\omega t = \alpha$ to π, $(2\pi+\alpha)$ to 3π etc…
- During this interval voltage across thyristor =0
- I is off from π to $(2\pi+\alpha)$, 3π to $(4\pi+\alpha)$ etc…
- During this interval voltage across thyristor has the wave shape of supply voltage

Single phase half wave circuit with R load



(a) Circuit diagram
(b) Waveforms

Fig. 10.1: Single phase fully controlled half wave rectifier supplying a resistive load

Single phase half wave circuit with R load

It may be observed that $v_s = v_o + v_T$

As the thyristor is reverse biased for π *radians, circuit turn off time*

$t_c = \frac{\pi}{\omega}$, *where* $\omega = 2\pi f$ *and* f *is the supply frequency*

Average voltage across load R is given by

$$V_o = \frac{1}{2\pi}\int_{\alpha}^{\pi} V_m \sin\omega t.\, d(\omega t) = \frac{V_m}{2\pi}(1+\cos\alpha)$$

The maximum value of average output voltage occurs at $\alpha = 0$

$$V_{o.m} = \frac{V_m}{2\pi}.2 = \frac{V_m}{\pi} \qquad Also, V_o = \frac{V_{o.m}}{2}(1+\cos\alpha)$$

Single phase half wave circuit with R load

$$Average\ load\ current, I_o = \frac{V_o}{R} = \frac{V_m}{2\pi R}(1+\cos\alpha)$$

- R.m.s. value of voltage is given by

$$V_{or} = \left[\frac{1}{2\pi}\int_{\alpha}^{\pi} {V_m}^2 \sin^2\omega t.\, d(\omega t)\right]^{1/2}$$

$$= \frac{V_m}{2\sqrt{\pi}}\left[(\pi-\alpha)+\frac{1}{2}\sin 2\alpha\right]^{1/2}$$

- The value of r.m.s current is

$$I_{or} = \frac{V_{or}}{R}$$

- Power delivered to resistive load = (rms load voltage)(rms load current) $= V_{or}I_{or} = \frac{V_{or}^{\ 2}}{R} = I_{or}^{\ 2}R$

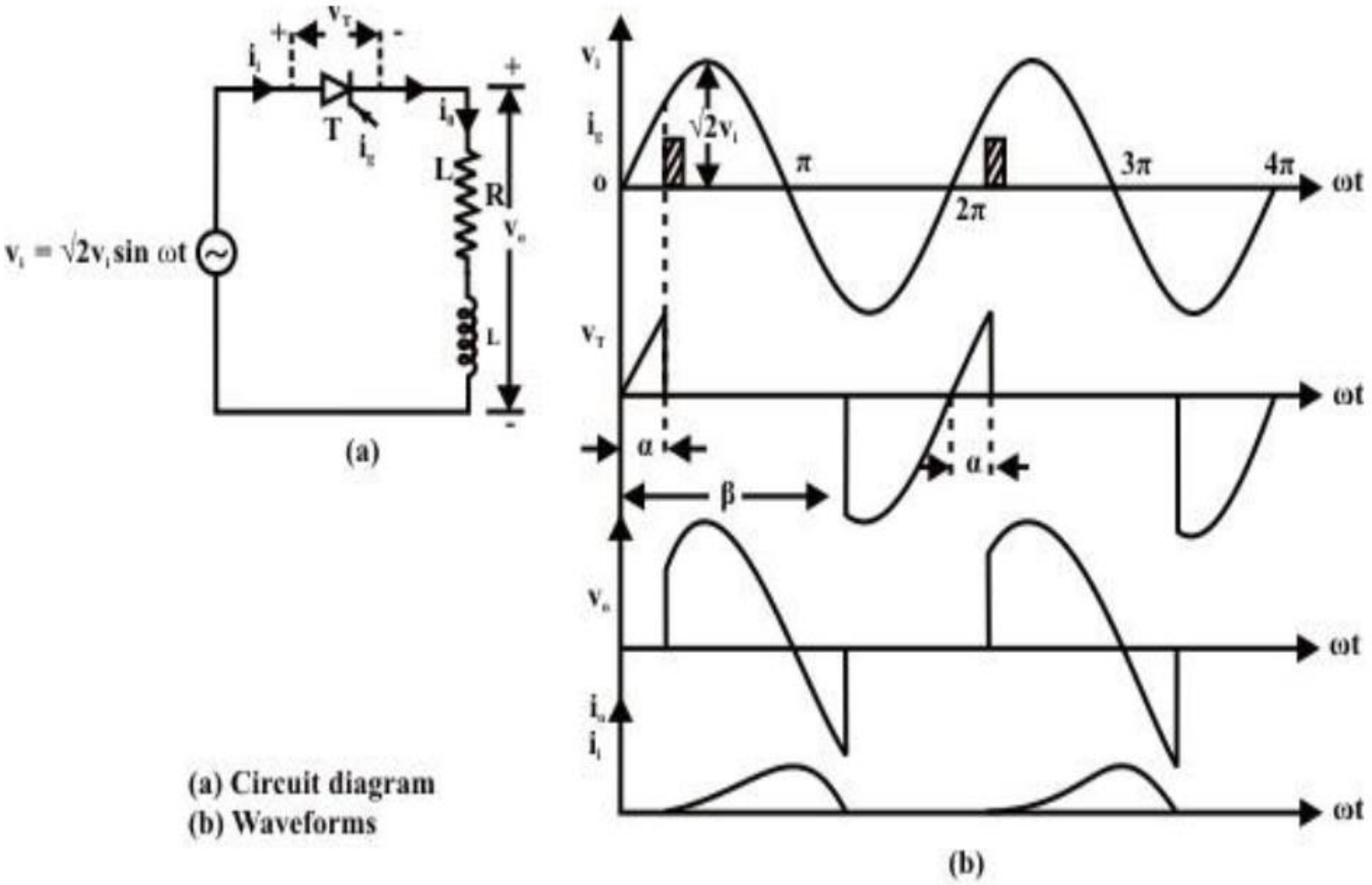
- Input volt amperes = (rms source voltage) (total rms line current) $= V_sI_{or} = \frac{V_s^{\ 2}\sqrt{2}}{2R\sqrt{\pi}}\left[(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right]^{1/2}$

- Input power factor

$$= \frac{power\ delivered\ to\ the\ load}{input\ VA} = \frac{V_{or}I_{or}}{V_sI_{or}} = \frac{V_{or}}{V_s}$$

$$pf = \frac{1}{\sqrt{2\pi}}\left[(\pi - \alpha) + \frac{1}{2}\sin 2\alpha\right]^{1/2}$$

Single phase half wave circuit with RL load



(a) Circuit diagram
(b) Waveforms

Fig. 10.2: Single phase fully controlled half wave rectifier supplying a resistive inductive load

- At $\omega t=\alpha$ thyristor is turned on by gate signal
- The load voltage Vo at once become equal to the source voltage Vs
- But the inductance L forced the load, or output current io to rise gradually
- After some time io reaches maximum value and then begin to decrease
- At $\omega t=\pi$, Vo is zero but io is not zero because of the load inductance
- After $\omega t=\pi$, SCR is subjected to reverse anode voltage but it will not be turned off as load current io is not less than holding current
- At some angle $\beta>\pi$, io reduces to zero and SCR is turned off as it is already reverse biased

- After $\omega t=\beta$, vo=0 and io=0
- At $\omega t=2\pi+\alpha$, SCR is triggered again, vo is applied to the load and load current develops as before
- Angle is called the extinction angle and is called the conduction angle
- The circuit turn off time $t_c = \frac{2\pi - \beta}{\omega}$
- The voltage equation for the circuit when T is on

$$V_m \sin \omega t = R i_o + L \frac{di}{dt}$$

- Average load voltage

$$V_0 = \frac{1}{2\pi}\int_{\alpha}^{\beta} V_m \sin\omega t.\, d(\omega t) = \frac{V_m}{2\pi}(\cos\alpha - \cos\beta)$$

- Average load current

$$I_o = \frac{V_m}{2\pi R}(\cos\alpha - \cos\beta)$$

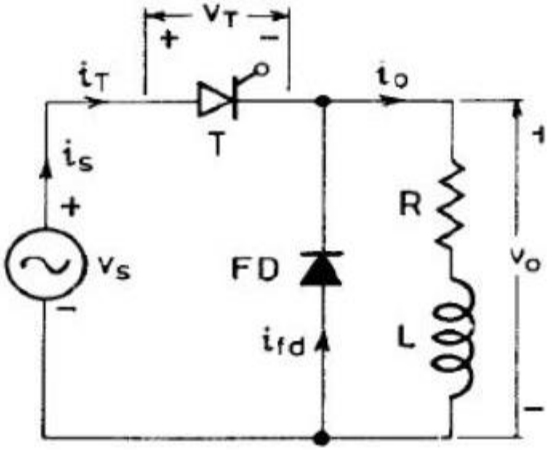
- Rms load voltage

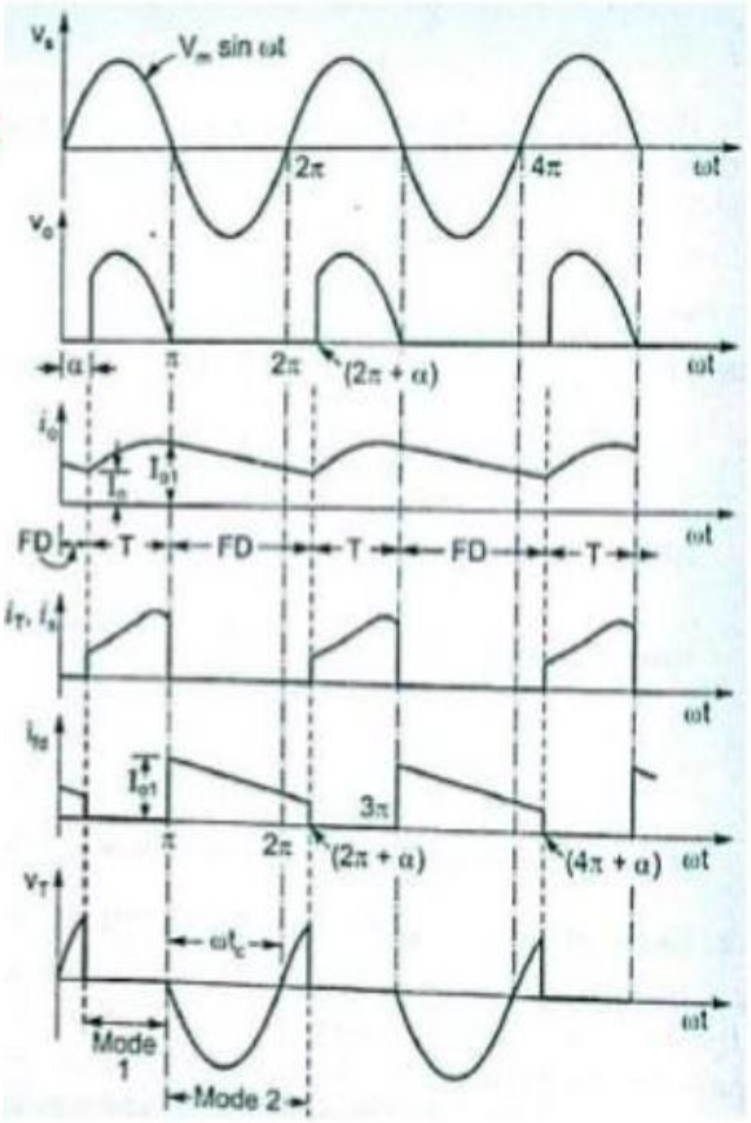
$$V_{or} = \left[\frac{1}{2\pi}\int_{\alpha}^{\beta} {V_m}^2 \sin^2\omega t.\, d(\omega t)\right]^{1/2}$$

$$= \frac{V_m}{2\sqrt{\pi}}\left[(\beta - \alpha) - \frac{1}{2}\{\sin 2\beta - \sin 2\alpha\}\right]^{1/2}$$

Single phase half wave circuit with RL load and freewheeling diode

Single phase Half wave Control with
R-L load & Free Wheeling Diode





- The waveform of load current io can be improved by connecting a freewheeling diode across the load
- A freewheeling diode is also called bypass diode or commutating diode
- At $\omega t=0$, source voltage becoming +ve
- At some delay angle α, forward biased SCR is triggered and source voltage Vs appears across the load as Vo
- At $\omega t=\pi$, source voltage Vs=0, and just after this instant as Vs tends to reverse freewheeling diode FD is forward biased through the conducting SCR
- As a result load current io is immediately transferred from SCR to FD as Vs tends to reverse

- At the same time SCR is subjected to reverse voltage and zero current, it is therefore turned off at $\omega t=\pi$
- It is assumed that during freewheeling period, load current does not decays to zero until the SCR is triggered again at $(2\pi+\alpha)$
- Voltage drop across FD is taken as almost zero, the load voltage vo is therefore zero during the freewheeling period
- SCR is reverse biased from $\omega t=\pi$ to $\omega t=2\pi$
- Therefore circuit turn off time

$$t_c = \frac{\pi}{\omega}$$

- Operation of the circuit can be explained in two modes
- *First mode – conduction mode*
- SCR conduct from α to π, $2\pi+\alpha$ to 3π and so on and FD is reverse biased
- The duration of this mode is for $[(\pi-\alpha)/\omega]$ sec
- For conduction mode the voltage equation be

$$V_m \sin \omega t = R i_o + L \frac{di_o}{dt}$$

- *Mode II – freewheeling mode*
- Π to $2\pi+\alpha$, 3π to $4\pi+\alpha$ etc...
- In this mode SCR is reverse biased from Π to 2π, 3π to 4π etc...

- As the load current is assume continues, FD conducts from Π to 2π+α, 3π to 4π+α etc... and so on
- The voltage equation for this mode

$$0 = Ri_o + L\frac{di_o}{dt}$$

- Average load voltage is given by

$$V_0 = \frac{1}{2\pi}\int_{\alpha}^{\pi} V_m \sin\omega t.d(\omega t) = \frac{V_m}{2\pi}(1+\cos\alpha)$$

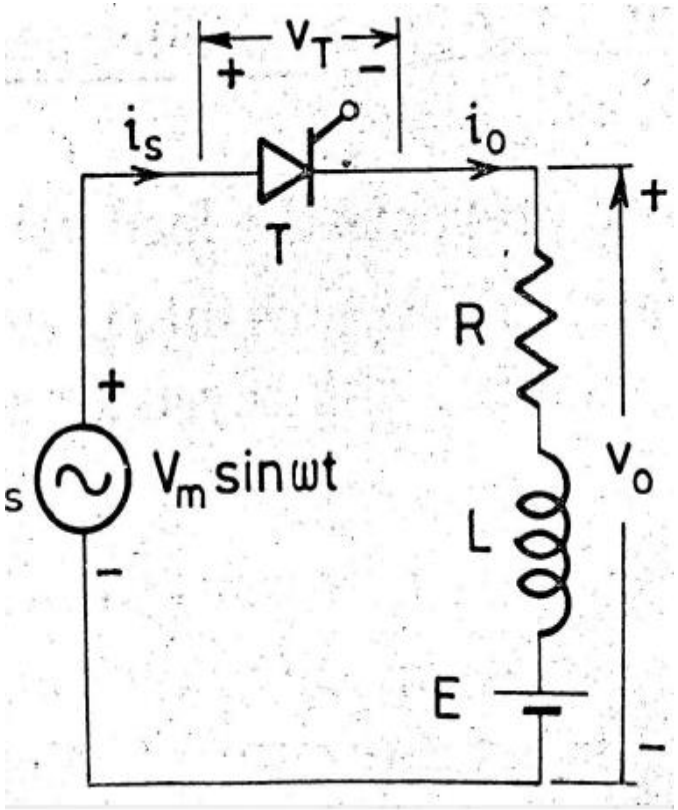
- Average load current

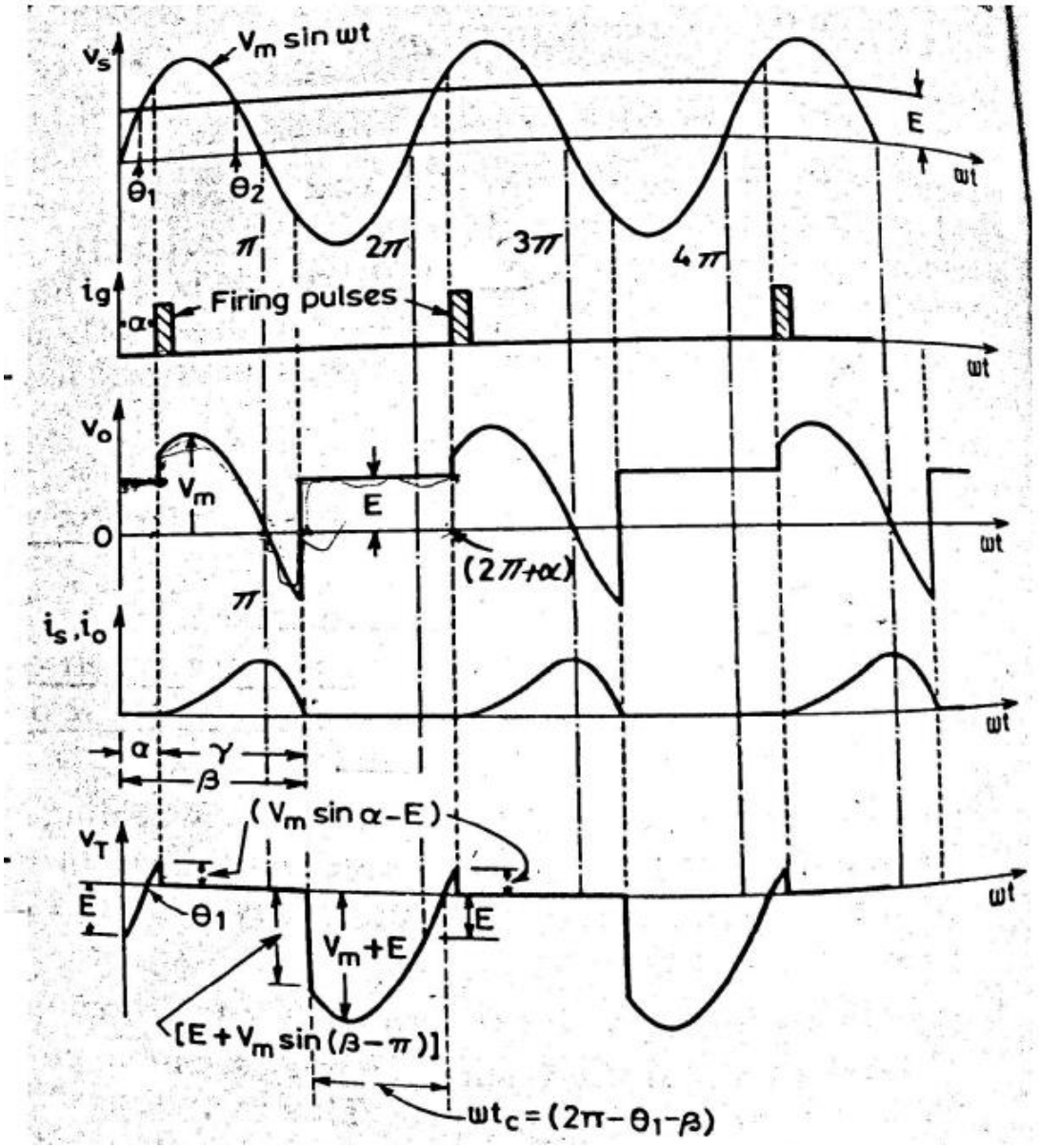
$$I_o = \frac{V_0}{R} = \frac{V_m}{2\pi R}(1+\cos\alpha)$$

The advantages of using FD are

- Input pf is improved
- Load current waveform is improved
- Load performance is better
- As energy is stored in the inductor L is transferred to R during the freewheeling period overall converter efficiency improves

Single phase half wave circuit with RLE load





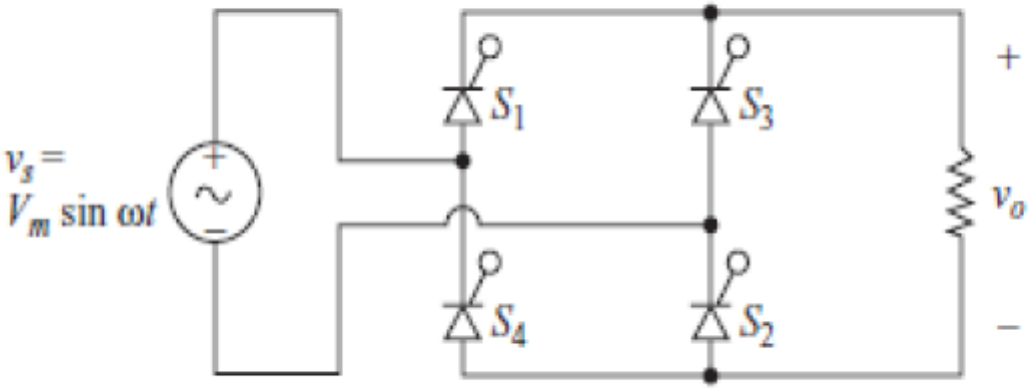
- The counter emf in the load may be due to battery or dc motor
- The minimum value of firing angle is obtained form the relation $V_m \sin \omega t = E$
- This is occur at an angle $\theta_1 = \sin^{-1}\left(E/V_m\right)$
- In case thyristor T is fired at an angle $\alpha < \theta_1$, then E>Vs, SCR is reverse biased and therefore it will not turn on
- Similarly maximum value of firing angle is $\theta_2 = \pi - \theta_1$
- During the interval load current is zero and load voltage V0=E
- And during the time io not zero, vo follows vs

- Voltage equation $V_m \sin \omega t = R i_o + L \frac{di_o}{dt} + E$
- $$V_0 = \frac{1}{2\pi} \int_{\alpha}^{\beta} V_m \sin \omega t . d(\omega t) + E(2\pi + \alpha - \beta)$$

$$= \frac{1}{2\pi} [V_m(\cos \alpha - \cos \beta) + E(2\pi + \alpha - \beta)]$$

- Average load current $I_o = \frac{1}{2\pi R} [V_m(\cos \alpha + \cos \theta_1) - E(\pi - (\theta_1 + \alpha))]$

Single phase fully controlled bridge rectifier with R load



- The output voltage waveform for a controlled full-wave rectifier with a resistive load is shown in Fig.
- The average component of this waveform is determined from

$$V_o = \frac{1}{\pi}\int_{\alpha}^{\pi} V_m \sin(\omega t)\, d(\omega t) = \frac{V_m}{\pi}(1 + \cos\alpha)$$

- Average output current

$$I_o = \frac{V_o}{R} = \frac{V_m}{\pi R}(1 + \cos\alpha)$$

- Rms value of output voltage

$$V_{or} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi} {V_m}^2 \sin^2\omega t.\, d(\omega t)\right]^{1/2} = \left[\frac{{V_m}^2}{2\pi}[(\pi - \alpha) + (1 + \cos 2\alpha)]\right]^{1/2}$$

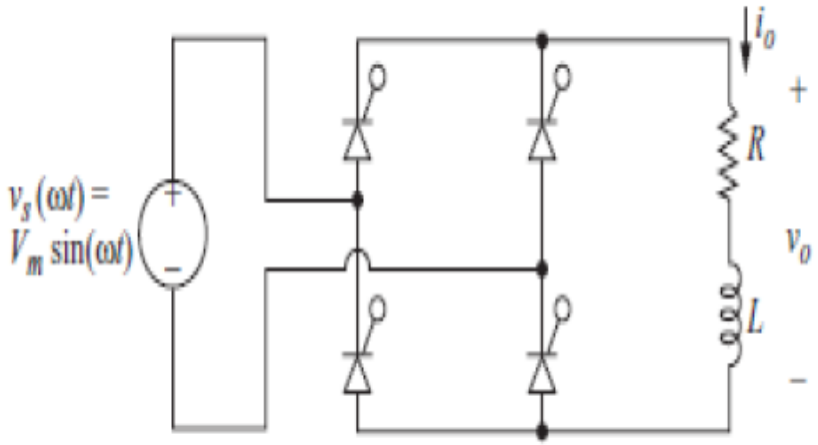
- The power delivered to the load is a function of the input voltage, the delay angle, and the load components; $P = I^2$ rms R *is used to determine the power in a* resistive load, where

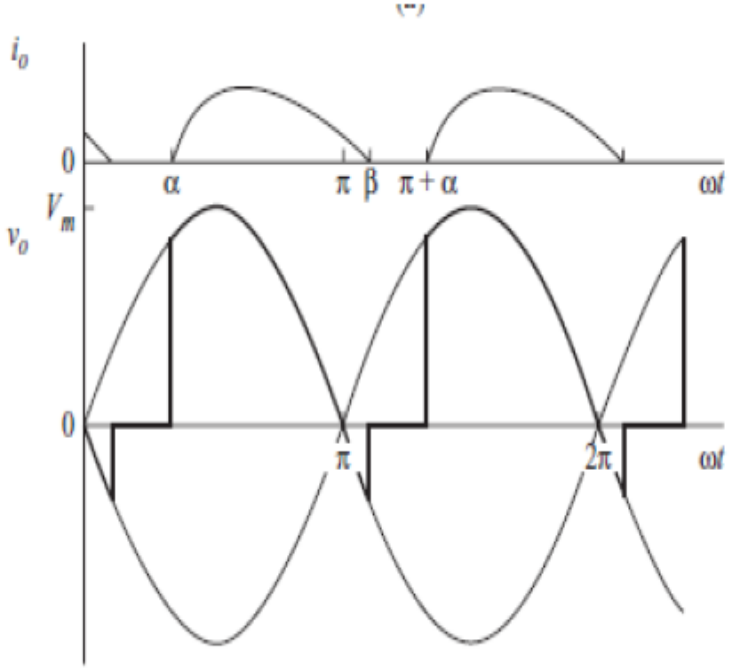
$$I_{\text{rms}} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi}\left(\frac{V_m}{R}\sin\omega t\right)^2 d(\omega t)}$$

$$= \frac{V_m}{R}\sqrt{\frac{1}{2} - \frac{\alpha}{2\pi} + \frac{\sin(2\alpha)}{4\pi}}$$

Single phase fully controlled bridge rectifier with RL load

Discontinues conduction





- Load current for a controlled full-wave rectifier with an RL load can be either continuous or discontinuous, and a separate analysis is required for each.
- Starting the analysis at $\omega t = 0$ with zero load current, SCRs S1 and S2 in the bridge rectifier will be forward-biased and S3 and S4 will be reverse-biased as the source voltage becomes positive.
- Gate signals are applied to S1 and S2 at $\omega t = \alpha$, turning S1 and S2 on.
- With S1 and S2 on, the load voltage is equal to the source voltage.

- Current function

$$i_o(\omega t) = \frac{V_m}{Z}\left[\sin(\omega t - \theta) - \sin(\alpha - \theta)\, e^{-(\omega t - \alpha)/\omega\tau}\right] \quad \text{for } \alpha \le \omega t \le \beta$$

where (4-26)

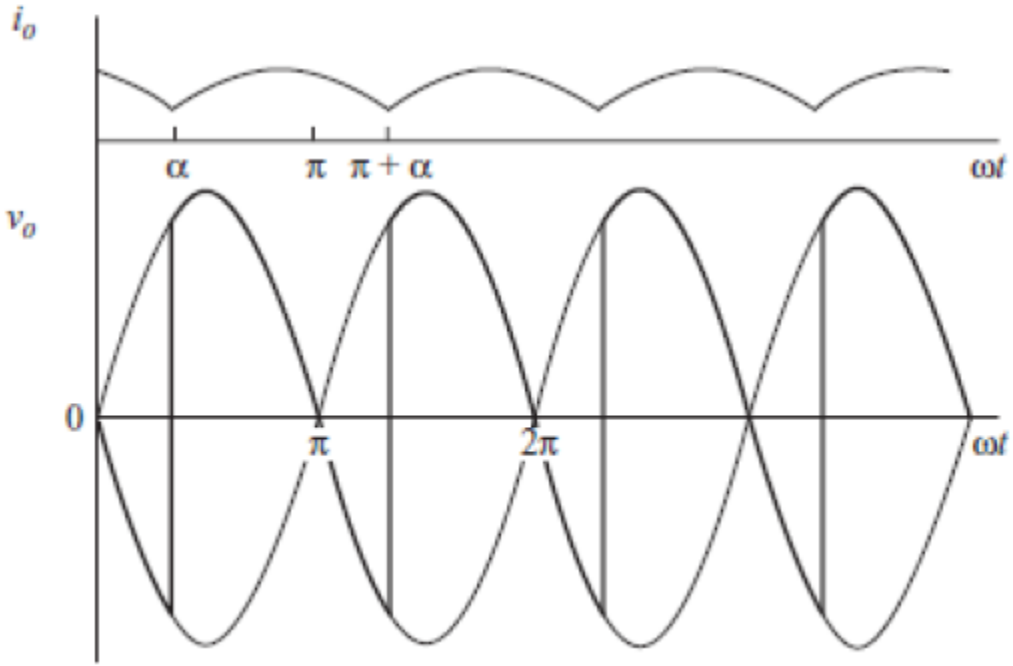
$$Z = \sqrt{R^2 + (\omega L)^2} \qquad \theta = \tan^{-1}\left(\frac{\omega L}{R}\right) \qquad \text{and} \qquad \tau = \frac{L}{R}$$

- The above current function becomes zero at $\omega t = \beta$.
- If $\beta < \pi + \alpha$, the current remains at zero until $\omega t = \pi + \alpha$, when gate signals are applied to S3 and S4 which are then forward-biased and begin to conduct.
- This mode of operation is called discontinuous current, which is illustrated in Fig. b.

$$\beta < \alpha + \pi \rightarrow \text{discontinuous current}$$

Continues conduction

- If the load current is still positive at $\omega t=\pi+\alpha$, when gate signals are applied to S3 and S4 in the above analysis, S3 and S4 are turned on and S1 and S2 are forced off



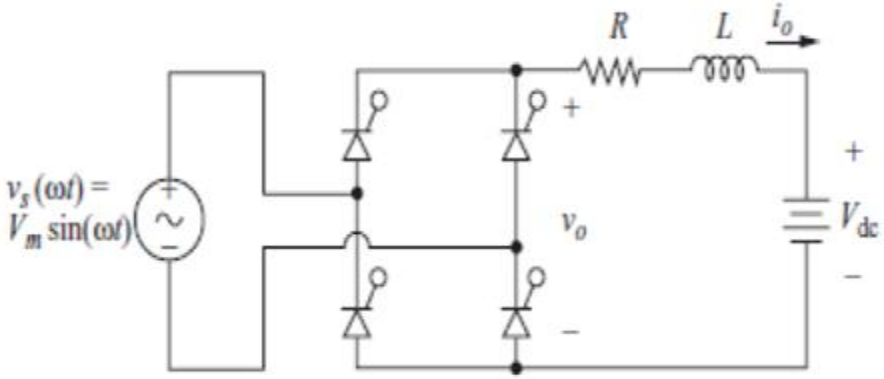
- Average output voltage

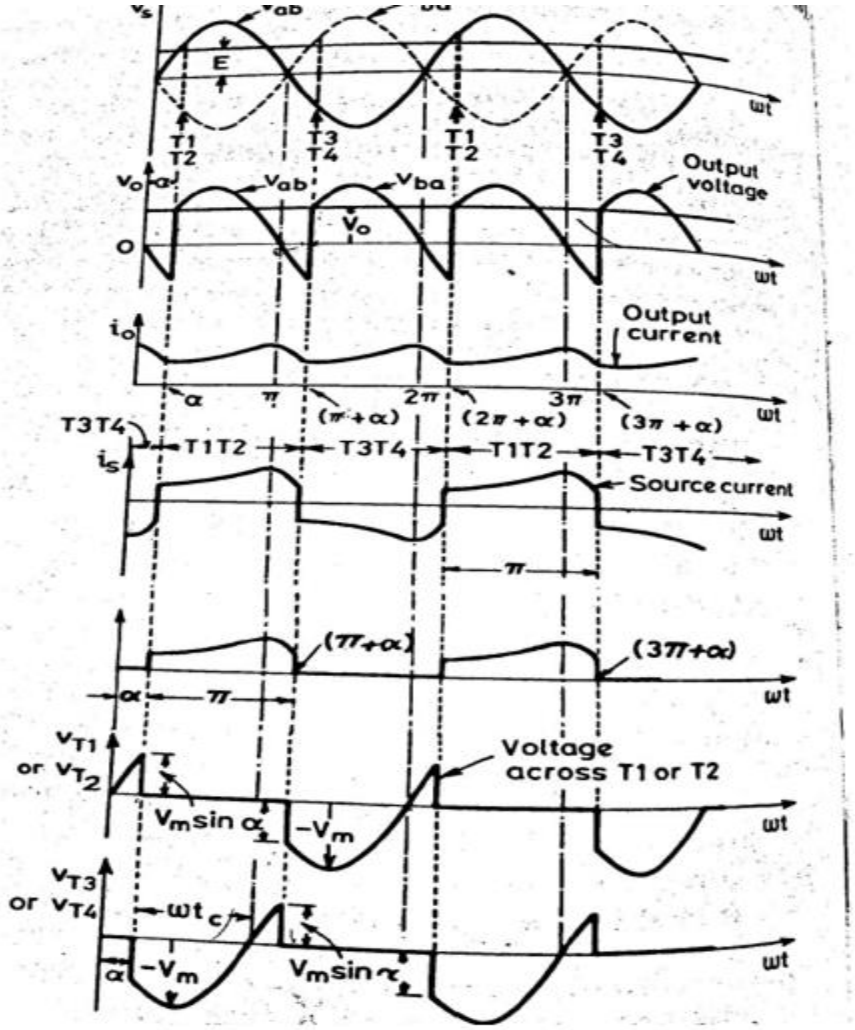
$$V_0 = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_m \sin\omega t.\, d(\omega t) = \frac{2V_m}{\pi}(\cos\alpha)$$

- Rms value of voltage

$$V_{or} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} {V_m}^2 \sin^2\omega t.\, d(\omega t)\right]^{1/2}$$

Single phase fully controlled bridge rectifier with RLE load





(Continues conduction)

- Average value of output voltage is given by

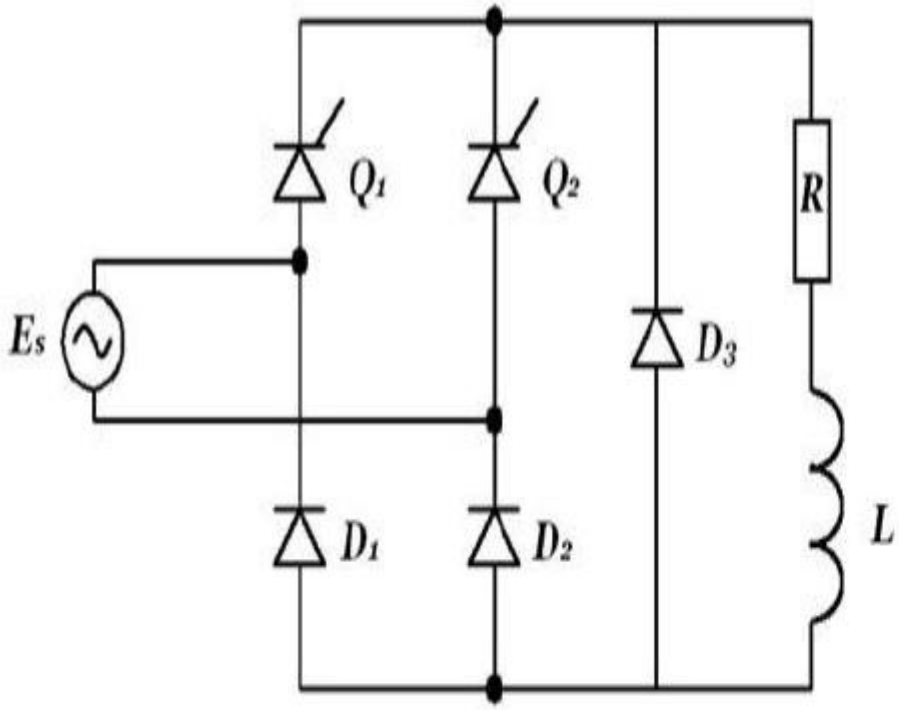
$$V_0 = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_m \sin\omega t.\, d(\omega t) = \frac{2V_m}{\pi}(\cos\alpha)$$

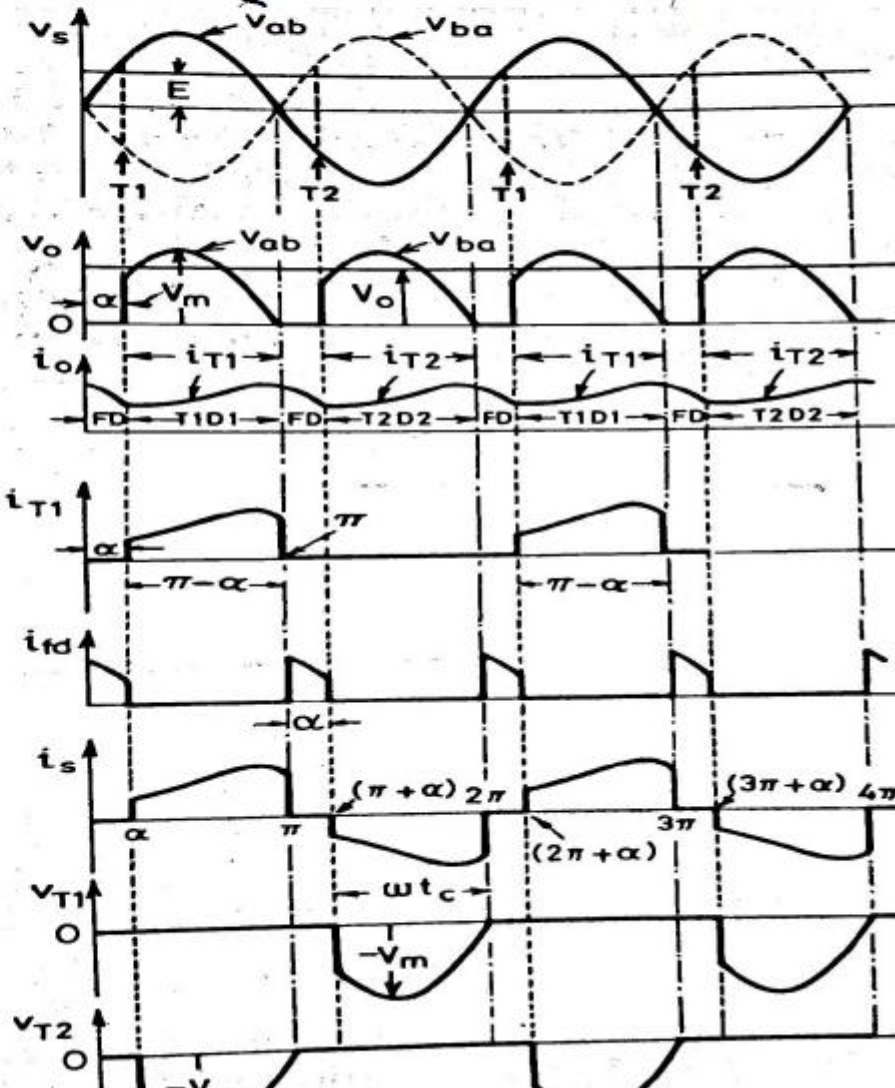
- Rms value (*square root of)

$$V_0 = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} {V_m}^2 \sin^2\omega t.\, d(\omega t) = \frac{{V_m}^2}{\pi}\left[\omega t - \frac{1}{2}|\sin 2\omega t|_{\alpha}^{\pi+\alpha}\right] = \frac{{V_m}^2}{2}$$

Single phase semi converter

- A single phase semi converter bridge with two thyristor a three diodes are shown





- The two thyristor are T1 and T2, and the two diode D1, D2 and third diode is connected across load as free wheeling diode
- The load is of RLE type
- After $\omega t=0$, thyristor T1 is forward biased only when source voltage exceeds E
- Thus T1 is triggered at a firing angle α, such that $V_m \sin\alpha > E$
- With T1 on load get connected to source through T1 and D1
- For the period $\omega t = \alpha$ to π, load current io flows through RLE load, D1, source and T1
- And the load terminal voltage is same as source voltage

- Soon after $\omega t=\pi$, load voltage Vo tends to reverse as the ac source voltage changes polarity
- Just as Vo tends to reverse, FD gets forward biased and starts conducting
- The load or output current io is transferred from T1, D1 to FD
- As T1 is reverse biased at $\omega t=\pi+$ through FD, T1 is turned off at $\omega t=\pi+$
- The load terminal are short circuited through FD therefore load or output voltage is zero during $\pi< \omega t< \pi+\alpha$
- After $\omega t= \pi$, during –ve half cycle, T2 will be forward biased only when the source voltage is more than E

- Semi converter with R load

$$V_0 = \frac{1}{\pi}\int_{\alpha}^{\pi} V_m \sin\omega t.\, d(\omega t) = \frac{V_m}{\pi}(1+\cos\alpha)$$

- Semi converter with RL load (continues conduction)

$$V_0 = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_m \sin\omega t.\, d(\omega t) = \frac{2V_m}{\pi}(\cos\alpha)$$

- Semi converter with RL load and free wheeling diode

$$V_0 = \frac{1}{\pi}\int_{\alpha}^{\pi} V_m \sin\omega t.\, d(\omega t) = \frac{V_m}{\pi}(1+\cos\alpha)$$

- Semi converter with RLE load (continues conduction)

$$V_0 = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_m \sin\omega t.\, d(\omega t) = \frac{2V_m}{\pi}(\cos\alpha)$$

- Semi converter with RLE load and free wheeling diode

$$V_0 = \frac{1}{\pi}\int_{\alpha}^{\pi} V_m \sin\omega t.\, d(\omega t) = \frac{V_m}{\pi}(1+\cos\alpha)$$

Module 3

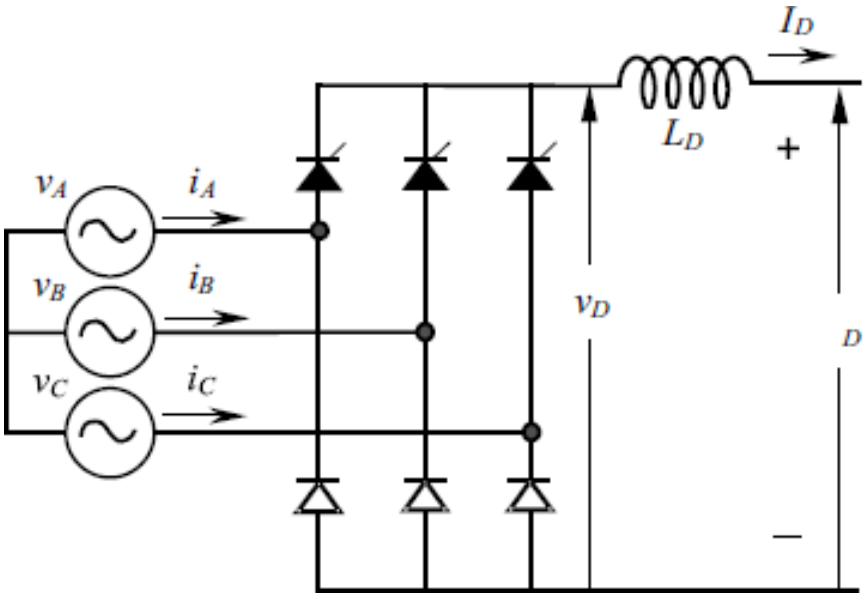
Module 3

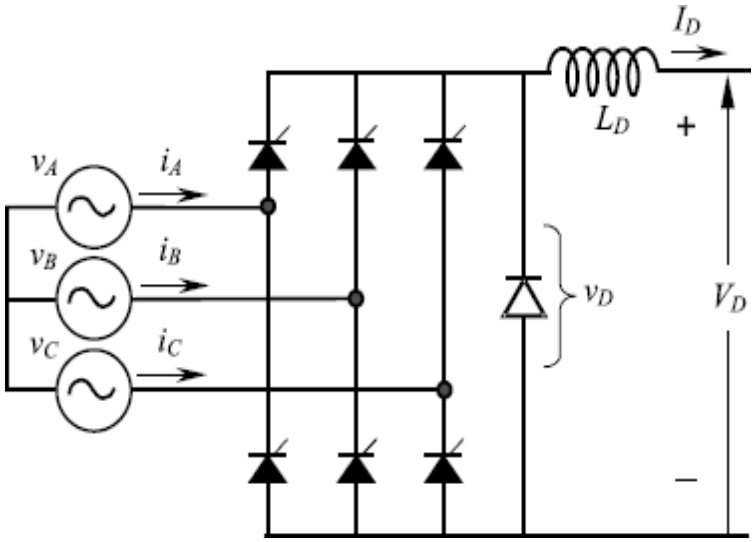
3-phase half-wave controlled rectifier with R load – 3-phase fully controlled & half-controlled converter with RLE load (continuous conduction, ripple free) – output voltage equation-waveforms for various triggering angles (no analysis) – 1-phase & 3-phase dual converter with & without circulating current – four-quadrantoperation

3 phase half-wave controlled rectifier with R load

- The half-controlled bridge, or „„semi-converter,“ is analyzed by considering it as a phase-controlled half-wave circuit in series with an uncontrolled half-wave rectifier.
- The average dc voltage is given by the following equation:

$$V_D = \frac{3 \cdot \sqrt{2} \cdot V_{f-f}^{\text{sec}}}{2\pi}(1 + \cos\alpha)$$



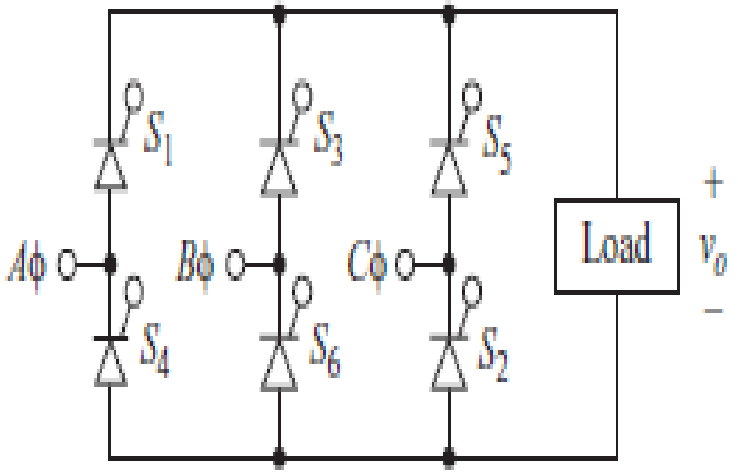


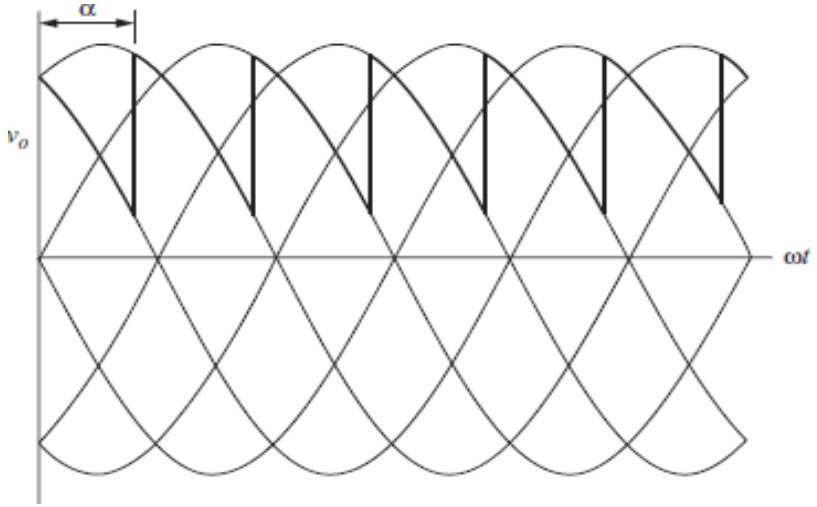
3 phase half-wave controlled rectifier with R load

- Then, the average voltage VD never reaches negative values.
- The output voltage waveforms of the half-controlled bridge are similar to those of a fully controlled bridge with a freewheeling diode.
- The advantage of the free-wheeling diode connection, shown in Fig is that there is always a path for the dc current independent of the status of the ac line and of the converter.
- This can be important if the load is inductive-resistive with a large time constant, and there is an interruption in one or more of the line phases.

3phasefullycontrolledrectifierwith RLE load

- The output of the three-phase rectifier can be controlled bysubstituting SCRs for diodes.
- Figure a shows a controlled six-pulse three-phase rectifier.
- With SCRs, conduction does not begin until a gate signal isapplied while the SCR isforward-biased.





3phasefullycontrolledrectifierwith RLE load

- Thus, the transition of the output voltage to the maximum instantaneous line-to-line source voltage can be delayed.
- The delay angle is referenced from where the SCR would begin to conduct if itwere a diode.
- The delay angle is the interval between when the SCR becomes forward-biased and when the gate signal is applied.
- Figure b shows the output of the controlled rectifier for adelay angle of 45.
- Average output voltage

$$V_0 = \frac{3}{\pi}\int_{\alpha+\pi/3}^{\alpha+2\pi/3} V_m \sin\omega t.d(\omega t) = \frac{3V_m}{\pi}(\cos\alpha)$$

Dual converters

- Semi-converters are single quadrant converters
- this means that over the entire firing angle range, load voltage and current have one polarity
- In full converters direction of current cannot reverse, because of the uni-directional property of the SCRs but polarity of output voltage can be reversed
- Thus a full converter operate as a rectifier in 1^{st} quadrant and as an inverter in 4^{th} quadrant.
- This shows that a full converter can operate as a two quadrant converter
- In the 1^{st} quadrant power flow from ac source to dc load and in 4^{th} quadrant power flow from dc crcuit to ac source

Dual converters

- In case four quadrant operation is required without any mechanical change over switch, two full converter can be connect back to back to the load circuit
- Such an arrangement using two full converters in anti- parallel and connected to the same dc load is known as a dual converter
- There are two functional modes of a dual converter Circulating current mode

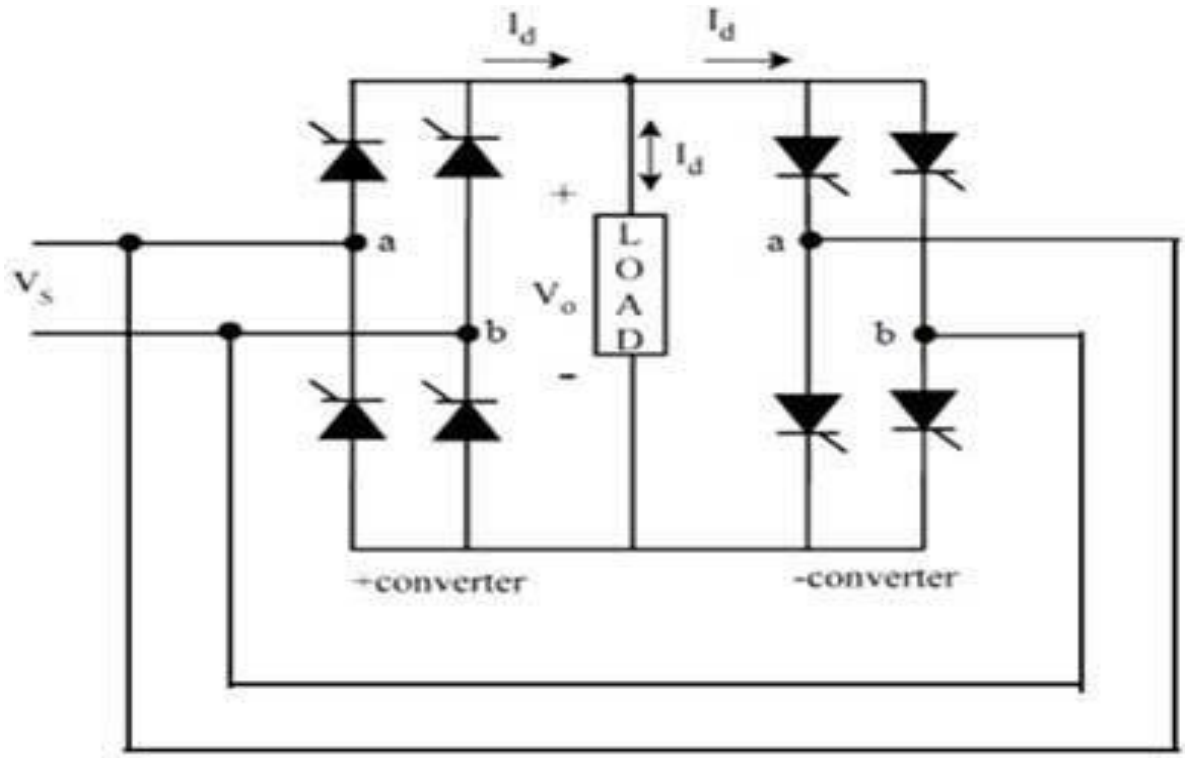
  Non-circulating current mode

Dualconverterwithoutcirculating current

- With non-circulating current dual converter, only one converter is in operation at a time and it alone carries the entire load current
- Only this converter receives the firing pulses from the trigger control
- The other converter is blocked from the conduction
- This is achieved by removing the firing pulses from this converter
- Thus only one converter is in operation at a time where as the other converter is idle

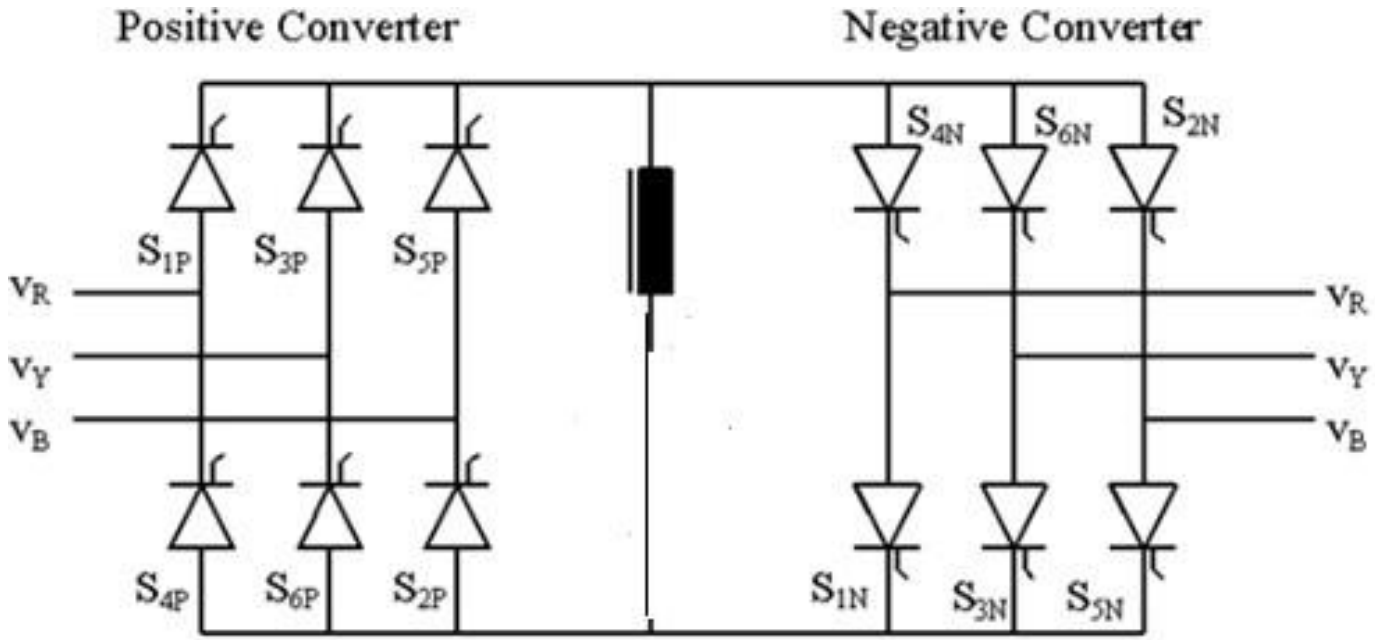
Dualconverterwithoutcirculating current

Single phase



Dualconverterwithoutcirculating current

Three phase



Dualconverterwithoutcirculating current

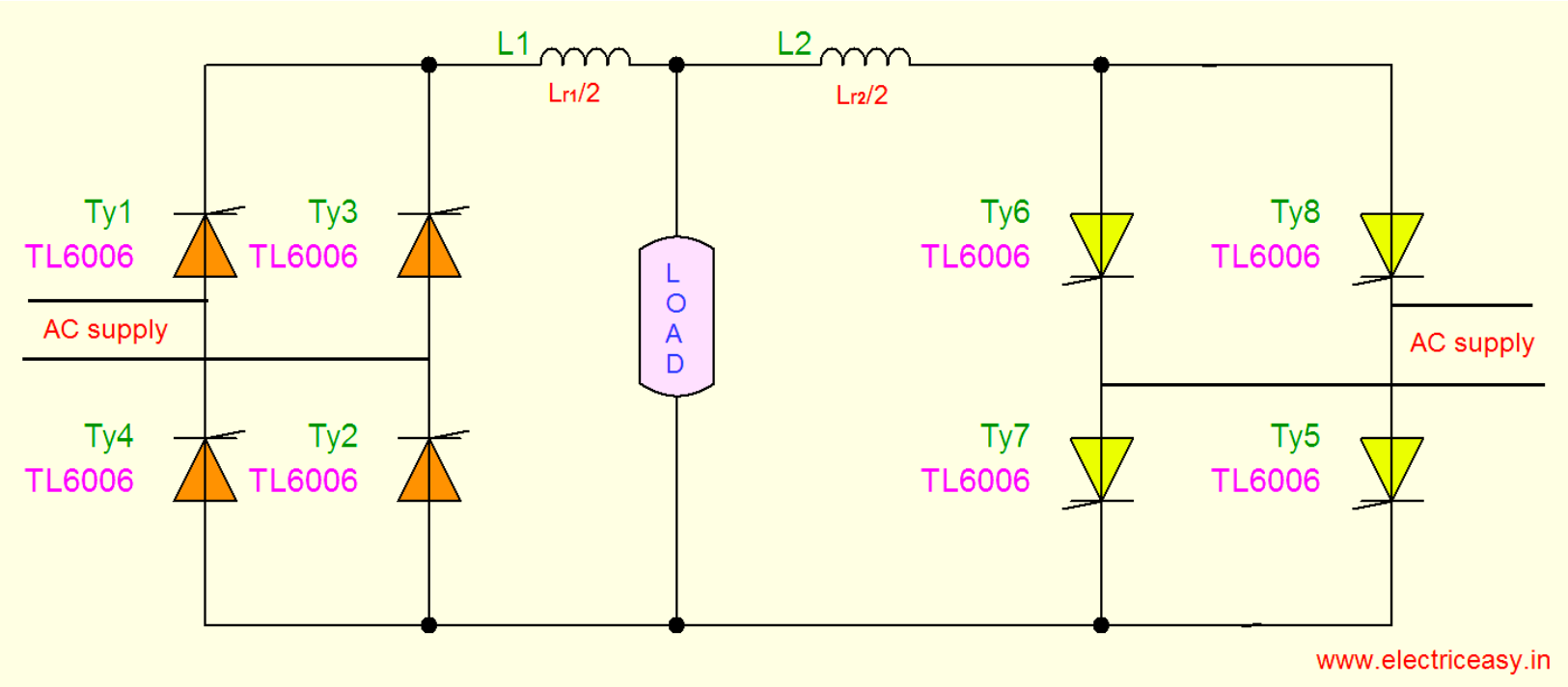
- Suppose converter 1 is in operation and is supplying the load current
- For blocking converter 1 and switching on converter 2, first firing pulses to converter 1 are immediately removed
- Or the firing angle of converter 1 is increased to maximum value and then its firing pulses are blocked
- With this load current would decay to zero and then only converter 2 is made to conduct by applying the firing pulses to it
- Now the current in converter 2 would build up through the load in the reverse direction
- As long as converter 2 is in operation converter 1 is idle asfiring pulses are withdrawn fromit

Dualconverterwithoutcirculating current

- It should be ensure that during changeover from one converter to another the load current must decays to zero
- After the outgoing conductor has stopped conducting, a delay time of 10 to 20 msec is introduced before the firing pulses are applied to switch on the incoming converter
- This time delay ensure reliable communication of SCRs in the outgoing converter
- If the incoming converter is triggered before the outgoing converter has been completely turned-off, a large circulating current would flow between two converters

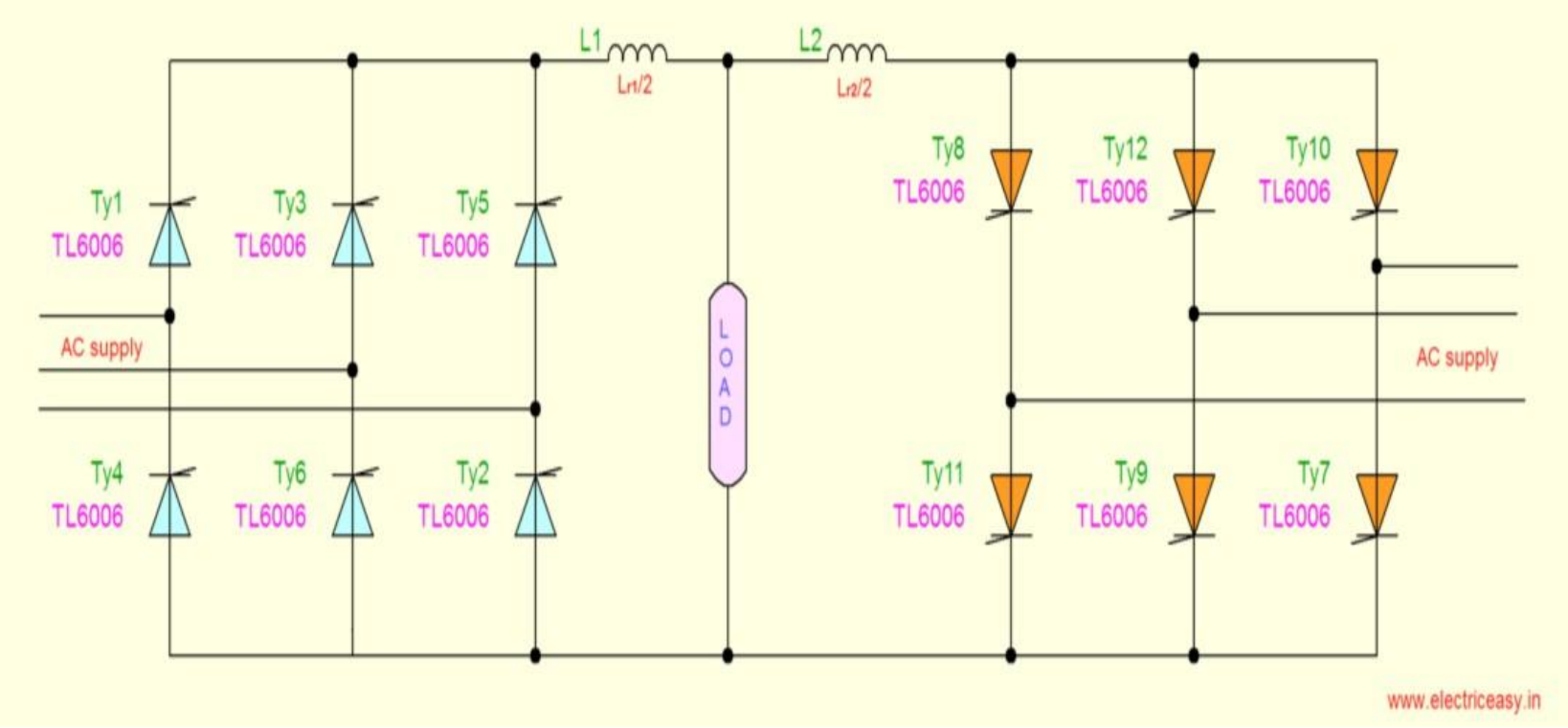
Dualconverterwithcirculatingcurrent

Single phase



Dualconverterwithcirculatingcurrent

Three phase



Dualconverterwithcirculatingcurrent

- In the circulating current mode of dual converter, a reactor is inserted in-between converter 1 and2
- This reactor limit the magnitude of circulating current to a reasonable value
- The firing pulses of the two converter is adjusted that=180
- If firing angle of converter 1 is 60 then firing angle of converter 2 is 120
- Therefore for these firing angle the converter 1 is working as rectifier and converter 2 asinverter
- Though the output voltage at terminals of both converter 1 and 2 has same polarity and also same average value
- However the instantaneous output voltage wave form is not similar

Dualconverterwithcirculatingcurrent

- As a consequence of it circulating current flows between two converters
- If the load current is to be reversed, the role of two converters is interchanged
- The main disadvantages of this converter are
  - A reactor is required to limit the circulating current
  - Circulating current give rise to more losses
  - As the converter has to handle load as well as circulating current the thyristor for the two converters are rated for higher current

Module 4

Module 4

Inverters – voltage source inverters– 1-phase half-bridge & full bridge inverter with R & RL loads – THD in output voltage – 3-phase bridge inverter with R load – 120° & 180° conduction mode – current source inverters.

Inverters

- Inverters are circuits that convert dc to ac. More precisely, inverters transfer power from a dc source to an ac load.
- Inverters are used in applications such as adjustable-speed ac motor drives, uninterruptible power supplies (UPS), and running ac appliances from an automobile battery.
- For sinusoidal ac outputs, the magnitude, frequency, and phase should be controllable. According to the type of ac output waveform, these topologies can be considered as
- voltage source inverters (VSIs),
- current source inverters (CSIs),

Voltage source inverters – single phase

- Single-phase voltage source inverters (VSIs) can be found as
  - half-bridge and
  - full-bridge topologies.
- Although the power range they cover is the low one, they are widely used in power supplies, single-phase UPSs, and currently to form elaborate high-power static power topologies, such as for instance, the multi-cell configurations

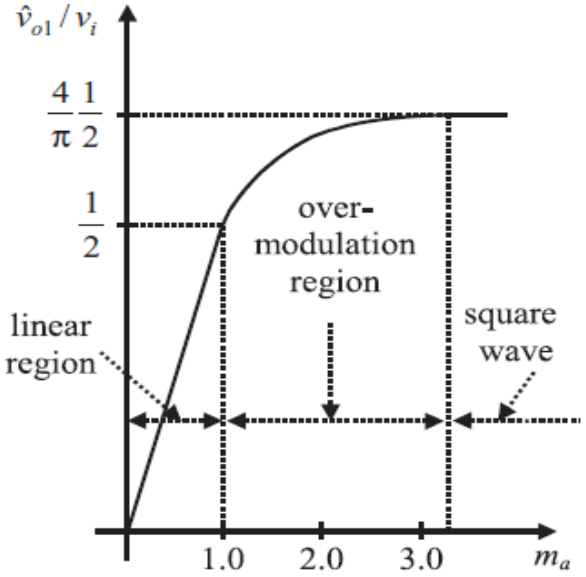
Single phase half bridge VSI

- Two large capacitors are required to provide a neutral point N, such that each capacitor maintains a constant voltage vi=2.
- Because the current harmonics injected by the operation of the inverter are low-order harmonics, a set of large capacitors (C+ and C-) is required.
- It is clear that both switches S+ and S- cannot be on simultaneously because a short circuit across the dc link voltage source vi would beproduced.

State	State	v	Components Conducting
+ is on and − is off	1	$v/2$	+ if >0
			+ if <0
− is on and + is off	2	$-v/2$	− if >0
			− if <0
+ and − are all off	3	$-v/2$	− if >0
		$v/2$	+ if <0

Single phase half bridge VSI

- There are two defined (states 1 and 2) and one undefined (state 3) switch state as shown in Table.
- In order to avoid the short circuit across the dc bus and the undefined ac output voltage condition, the modulating technique should always ensure that at any instant either the top or the bottom switch of the inverter leg is on.



Single phase half bridge VSI

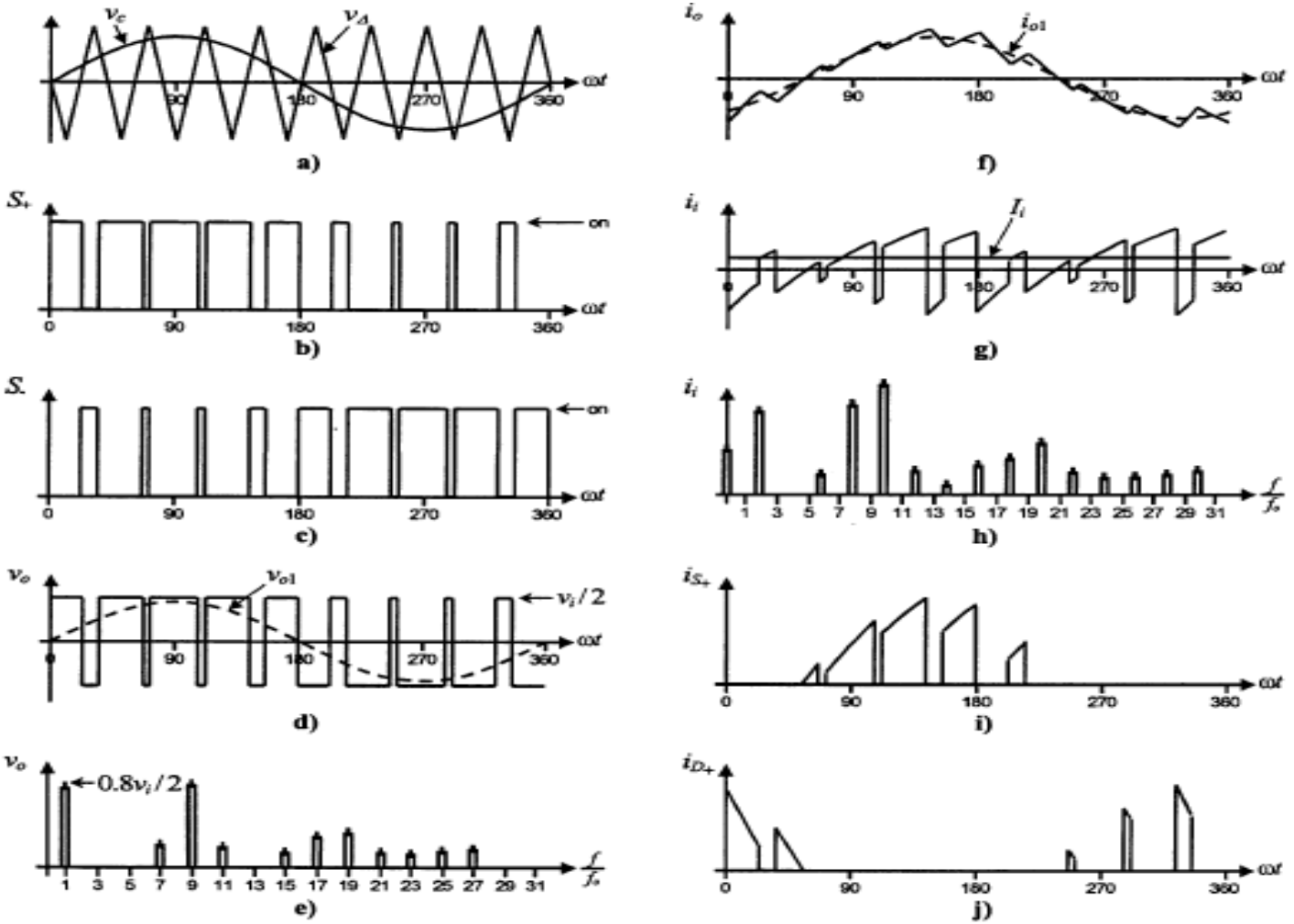
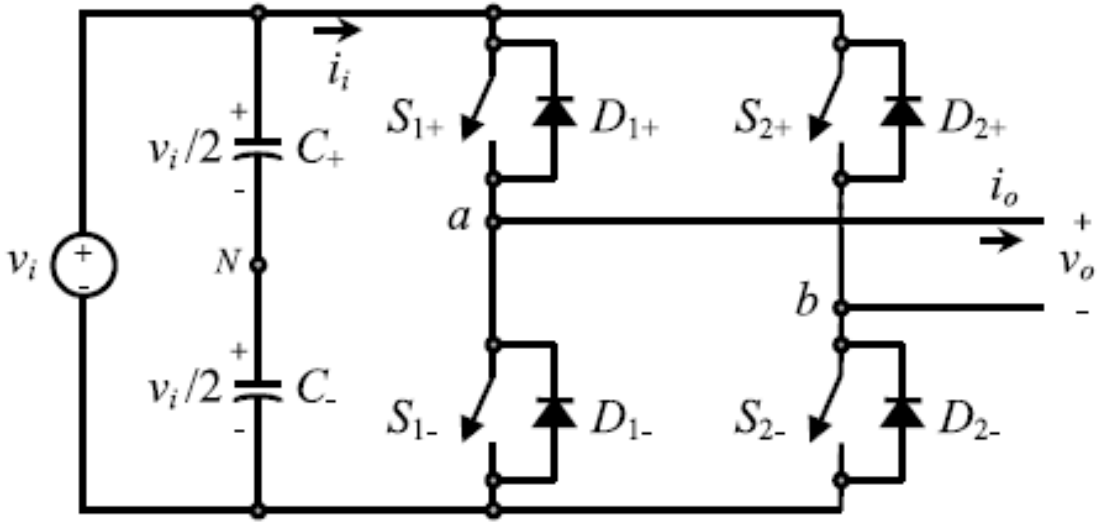


FIGURE 14.3 The half-bridge VSI. Ideal waveforms for the SPWM ($_a = 0.$, $=$): (a) carrier and modulating signals; (b) switch $_+$ state; (c) Switch $_-$ state; (d) ac output voltage; (e) ac output voltage spectrum; (f) ac output current; (g) dc current; (h) dc current spectrum; (i) switch $_+$ current; (j) diode $_+$ current.

Single phase full bridge VSI

- This inverter is similar to the half-bridge inverter; however, a second leg provides the neutral point to the load.
- As expected, both switches S1+ and S1- (or S2+ and S2-) cannot be on simultaneously because a short circuit across the dc link voltage source vi would be produced.



Single phase full bridge VSI

- There are four defined (states 1, 2, 3, and 4) and one undefined (state 5) switch states as shown in Table

State	State	v_a	v_b	v	Components Conducting	
$_{1+}$ and $_{2-}$ are on and $_{1-}$ and $_{2+}$ are off	1	$v/2$	$-v/2$	v	$_{1+}$ and $_{2-}$	if > 0
					$_{1+}$ and $_{2-}$	if < 0
$_{1-}$ and $_{2+}$ are on and $_{1+}$ and $_{2-}$ are off	2	$-v/2$	$v/2$	$-v$	$_{1-}$ and $_{2+}$	if > 0
					$_{1-}$ and $_{2+}$	if < 0
$_{1+}$ and $_{2+}$ are on and $_{1-}$ and $_{2-}$ are off	3	$v/2$	$v/2$	0	$_{1+}$ and $_{2+}$	if > 0
					$_{1+}$ and $_{2+}$	if < 0
$_{1-}$ and $_{2-}$ are on and $_{1+}$ and $_{2+}$ are off	4	$-v/2$	$-v/2$	0	$_{1-}$ and $_{2-}$	if > 0
					$_{1-}$ and $_{2-}$	if < 0
$_{1-}$, $_{2-}$, $_{1+}$, and $_{2+}$ are all off	5	$-v/2$	$v/2$	$-v$	$_{1-}$ and $_{2+}$	if > 0
		$v/2$	$-v/2$	v	$_{1+}$ and $_{2-}$	if < 0

Single phase full bridge VSI

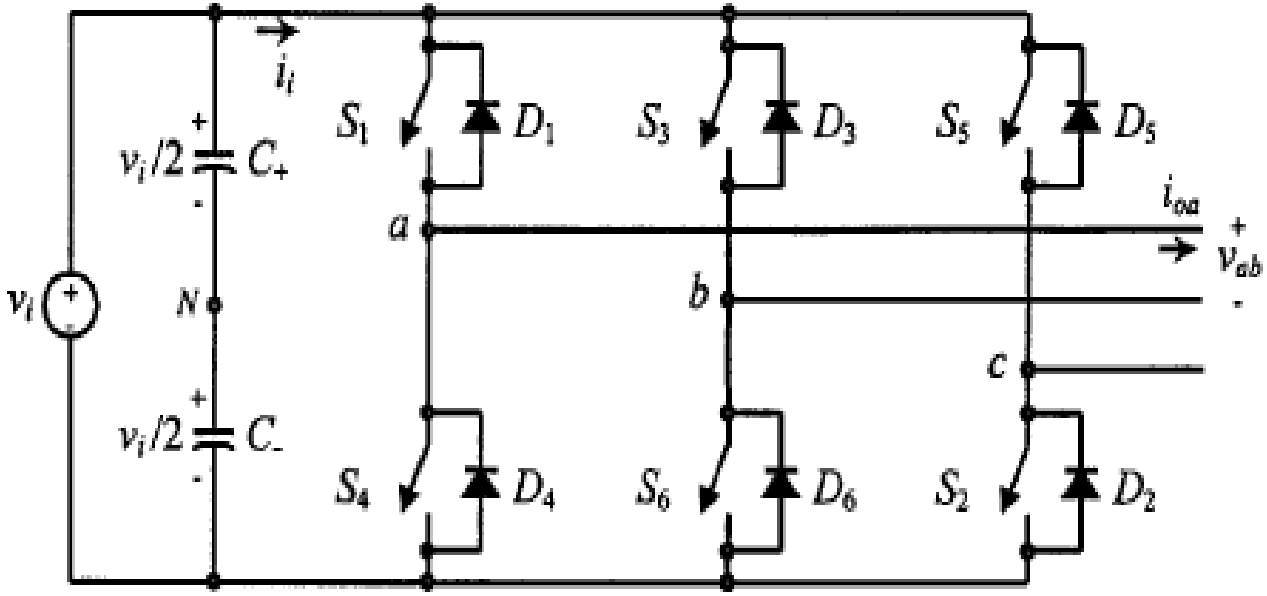
- The undefined condition should be avoided so as to be always capable of defining the ac output voltage.
- In order to avoid the short circuit across the dc bus and the undefined ac output voltage condition, the modulating technique should ensure that either the top or the bottom switch of each leg is on at any instant.
- It can be observed that the ac output voltage can take values up to the dc link value vi , which is twice that obtained with half-bridge VSI topologies.
- Several modulating techniques have been developed that are applicable to full-bridge VSIs.
- Among them are the PWM (bipolar and unipolar) techniques

Three phase bridge inverter

- Single-phase VSIs cover low-range power applications and three-phase VSIs cover the medium- to high-power applications.
- The main purpose of these topologies is to provide a three-phase voltage source, where the amplitude, phase, and frequency of the voltages should always be controllable.
- Although most of the applications require sinusoidal voltage waveforms (e.g., ASDs, UPSs, FACTS, var compensators),
- Arbitrary voltages are also required in some emerging applications (e.g., active filters, voltage compensators).

Three phase bridge inverter

- The standard three-phase VSI topology is shown in Fig. and the eight valid switch states are given in Table



Three phase bridge inverter

- As in single-phase VSIs, the switches of any leg of the inverter (S1 and S4, S3 and S6, or S5 and S2) cannot be switched on simultaneously because this would result in a short circuit across the dc link voltage supply.

State	State	v_{ab}	v_b	v_a	Space Vector
1, 2, and 6 are on and 4, 5, and 3 are off	1	v	0	$-v$	$\mathbf{V}_1 = 1 + j0.5$
2, 3, and 1 are on and 5, 6, and 4 are off	2	0	v	$-v$	$\mathbf{V}_2 = j1.155$
3, 4, and 2 are on and 6, 1, and 5 are off	3	$-v$	v	0	$\mathbf{V}_3 = -1 + j0.5$
4, 5, and 3 are on and 1, 2, and 6 are off	4	$-v$	0	v	$\mathbf{V}_4 = -1 - j0.5$
5, 6, and 4 are on and 2, 3, and 1 are off	5	0	$-v$	v	$\mathbf{V}_5 = -j1.155$
6, 1, and 5 are on and 3, 4, and 2 are off	6	v	$-v$	0	$\mathbf{V}_6 = 1 - j0.5$
1, 3, and 5 are on and 4, 6, and 2 are off	7	0	0	0	$\mathbf{V}_7 = 0$
4, 6, and 2 are on and 1, 3, and 5 are off	8	0	0	0	$\mathbf{V}_8 = 0$

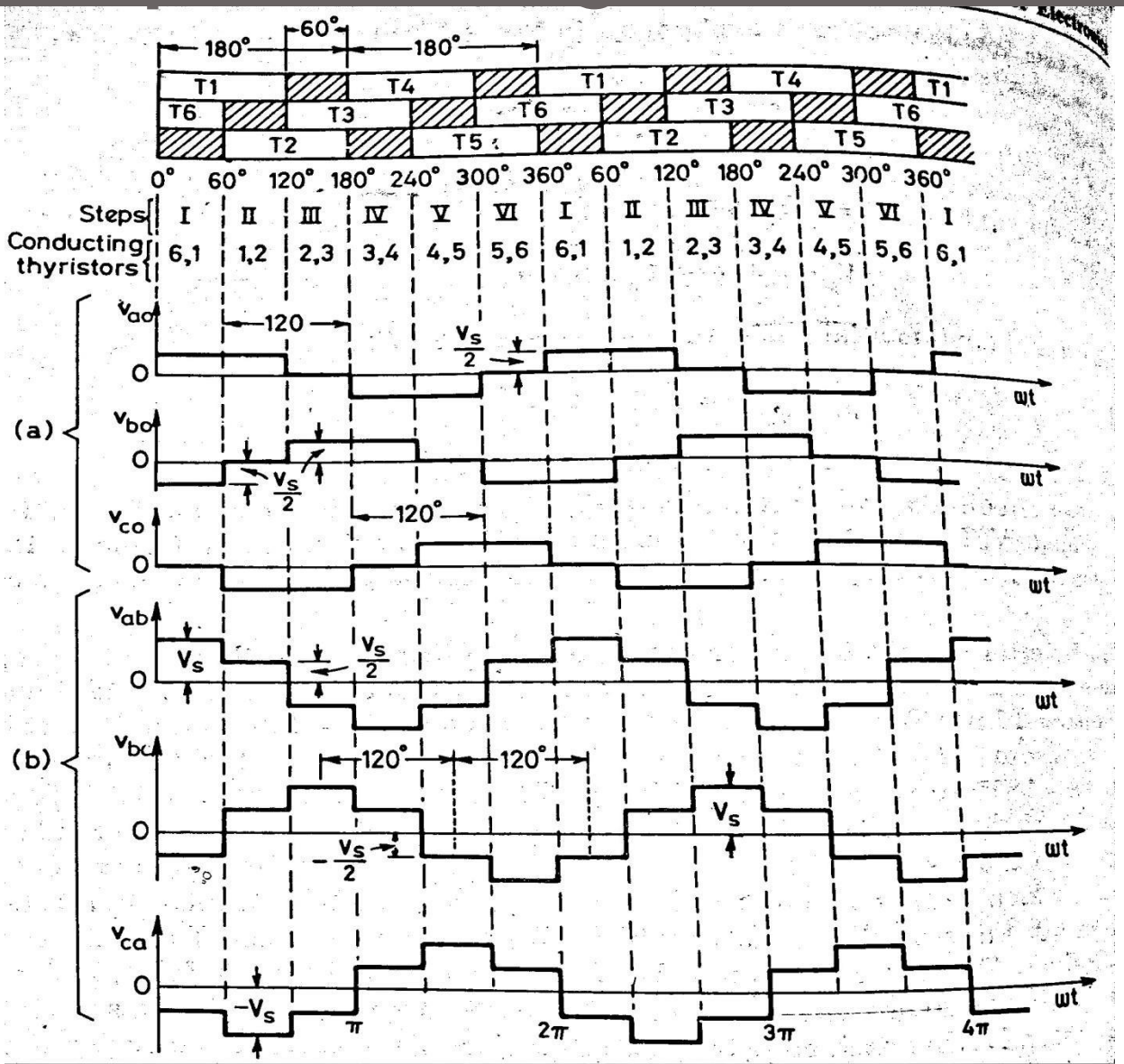
Three phase bridge inverter

- Similarly, in order to avoid undefined states in the VSI, and thus undefined ac output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously as this will result in voltages that will depend upon the respective line current polarity.
- The eight valid states, two of them (7 and 8 in Table) produce zero ac line voltages.
- In this case, the ac line currents freewheel through either the upper or lower components.

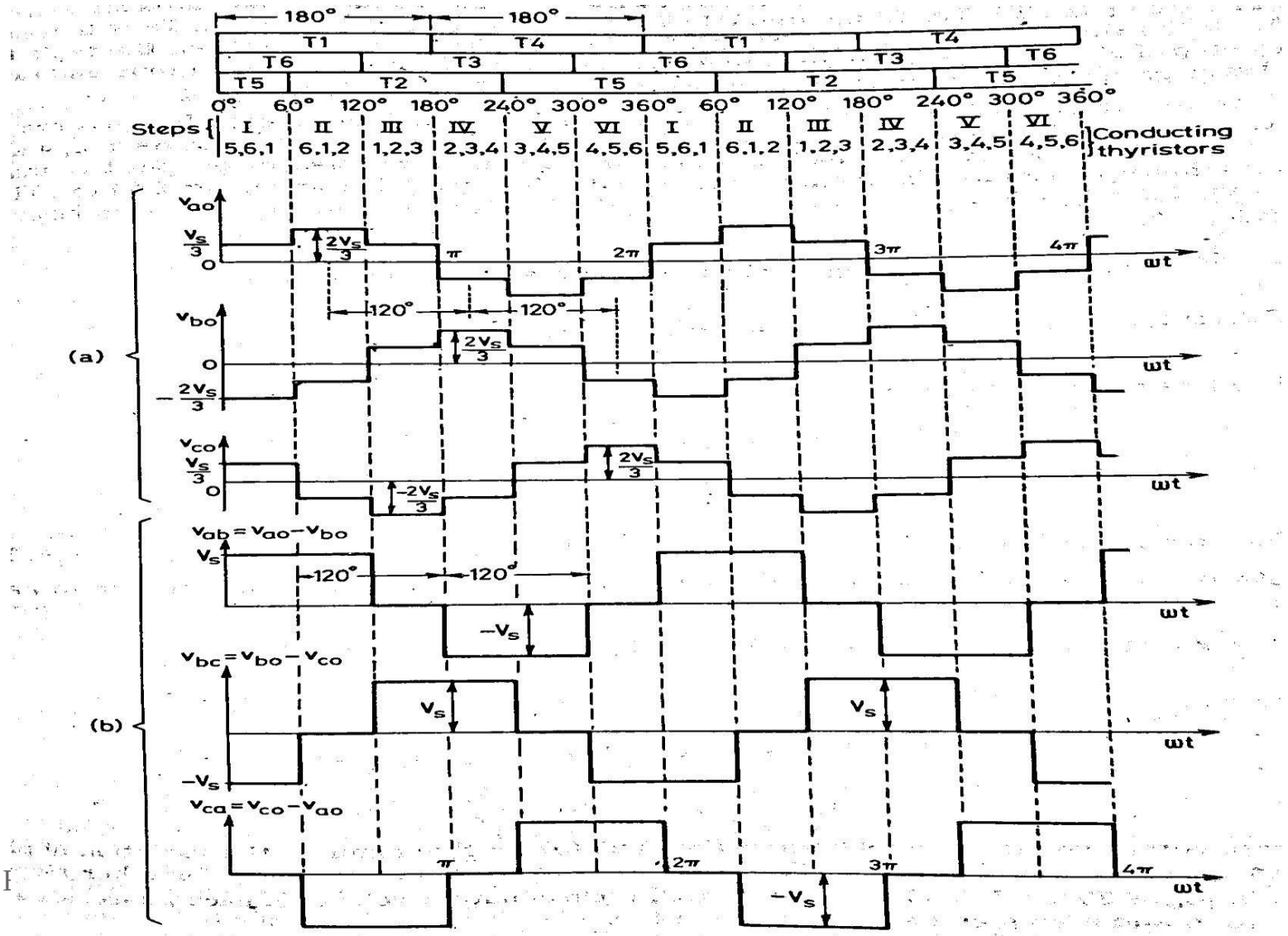
Three phase bridge inverter

- The remaining states (1 to 6 in Table) produce nonzero ac output voltages.
- In order to generate a given voltage waveform, the inverter moves from one state to another.
- Thus the resulting ac output line voltages consist of discrete values of voltages that are vi , 0, and -vi for the topology shown in Fig.
- The selection of the states in order to generate the give waveform is done by the modulating technique that should ensure the use of only the valid states.

Three phase bridge inverter – 120 ^{0}



Three phase bridge inverter – 180^0



Three phase bridge inverter

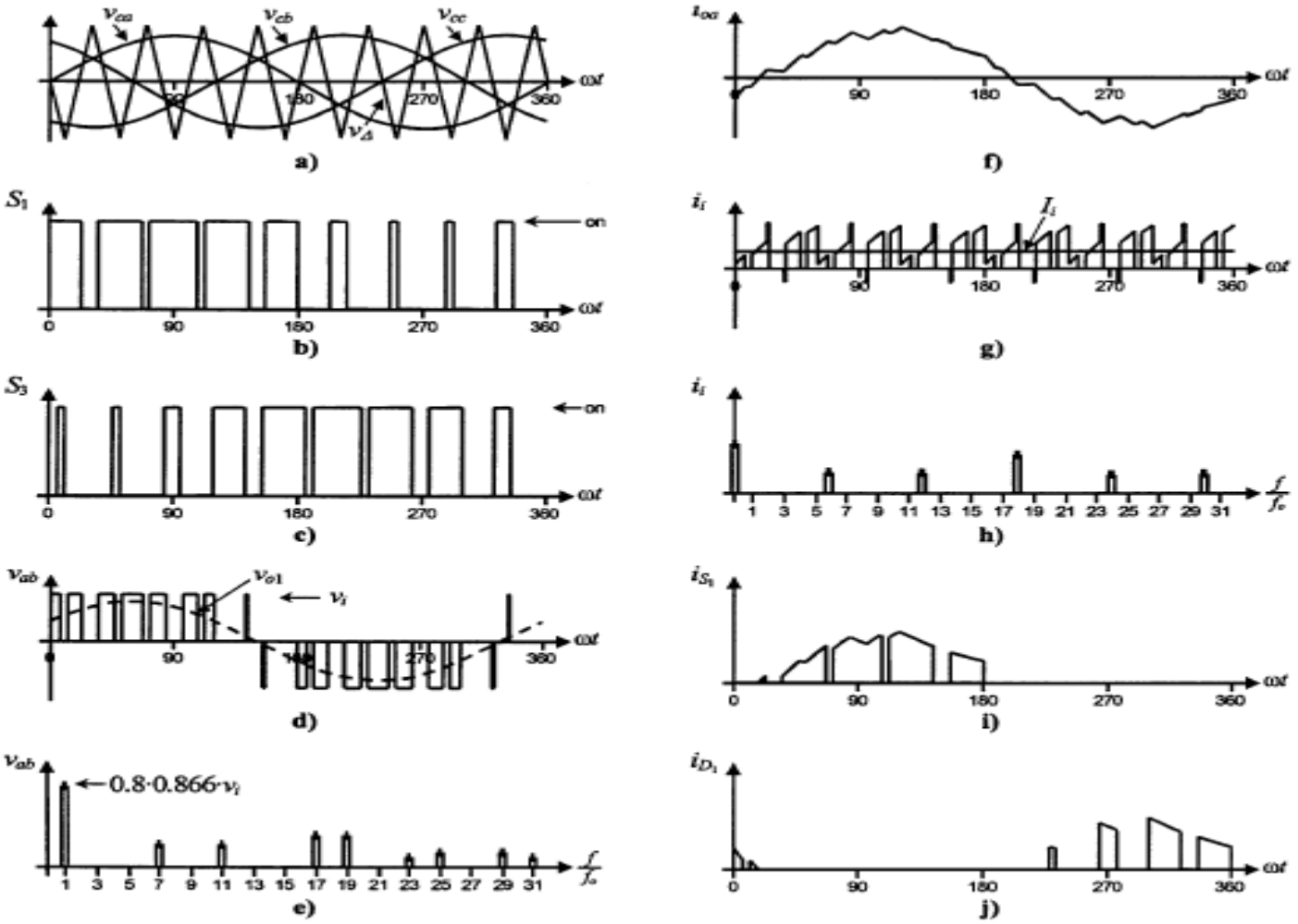
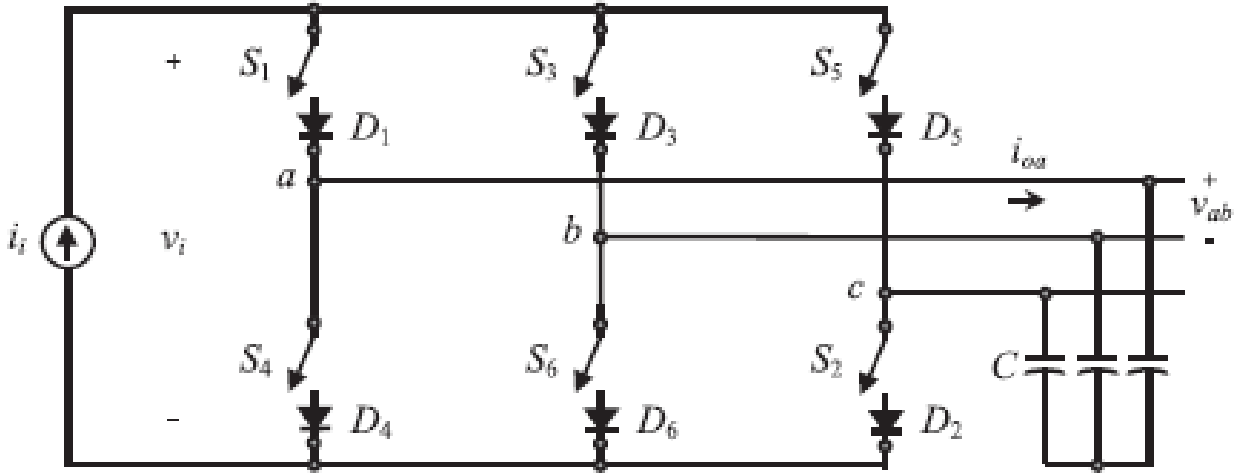


FIGURE 14.14 The three-phase VSI. Ideal waveforms for the SPWM ($_a = 0.$, $=$): (a) carrier and modulating signals; (b) switch $_1$ state; (c) switch $_3$ state; (d) ac output voltage; (e) ac output voltage spectrum; (f) ac output current; (g) dc current; (h) dc current spectrum; (i) switch $_1$ current; (j) diode $_1$ current.

Current source inverters

- The main objective of these static power converters is to produce ac output current waveforms from a dc current power supply.
- For sinusoidal ac outputs, its magnitude, frequency, and phase should be controllable.
- Due to the fact that the ac line currents ioa, iob, and ioc (Fig. CSI) feature high di=dt, a capacitive filter should be connected at the ac terminals in inductive load applications (such as ASDs).
- Thus, nearly sinusoidal load voltages are generated that justifies the use of these topologies in medium-voltage industrial applications, where high-quality voltage waveforms are required.
- Although single-phase CSIs can in the same way as three-phase CSIs topologies be developed under similar principles,

Current source inverters



State				State	a	b		Space Vector
$_1$ and $_2$ are on and	$_3$,	$_4$,	$_5$, and $_6$ are off	1		0	−	$\mathbf{I}_1 = 1 + j0.5$
$_2$ and $_3$ are on and	$_4$,	$_5$,	$_6$, and $_1$ are off	2	0		−	$\mathbf{I}_2 = j1.155$
$_3$ and $_4$ are on and	$_5$,	$_6$,	$_1$, and $_2$ are off	3	−		0	$\mathbf{I}_3 = -1 + j0.5$
$_4$ and $_5$ are on and	$_6$,	$_1$,	$_2$, and $_3$ are off	4	−	0		$\mathbf{I}_4 = -1 - j0.5$
$_5$ and $_6$ are on and	$_1$,	$_2$,	$_3$, and $_4$ are off	5	0	−		$\mathbf{I}_5 = -j1.155$
$_6$ and $_1$ are on and	$_2$,	$_3$,	$_4$, and $_5$ are off	6		−	0	$\mathbf{I}_6 = 1 - j0.5$
$_1$ and $_4$ are on and	$_2$,	$_3$,	$_5$, and $_6$ are off	7	0	0	0	$\mathbf{I}_7 = 0$
$_3$ and $_6$ are on and	$_1$,	$_2$,	$_4$, and $_5$ are off	8	0	0	0	$\mathbf{I}_8 = 0$
$_5$ and $_2$ are on and	$_6$,	$_1$,	$_3$, and $_4$ are off	9	0	0	0	$\mathbf{I}_9 = 0$

Current source inverters

- Only three-phase applications are of practical use and are analyzed in the following.
- In order to properly gate the power switches of a three phase CSI, two main constraints must always be met:

(a) the ac side is mainly capacitive, thus, it must not be short circuited; this implies that, at most one top switch (1, 3, or 5) and one bottom switch (4, 6, or 2) should be closed at any time; and

(b) the dc bus is of the current-source type and thus it cannot be opened; therefore, there must be at least one top switch (1, 3, or 5) and one bottom switch (4, 6, or 2) closed at all times.

- Note that both constraints can be summarized by stating that at any time, only one top switch and one bottom switch must be closed.
- There are nine valid states in three-phase CSIs.

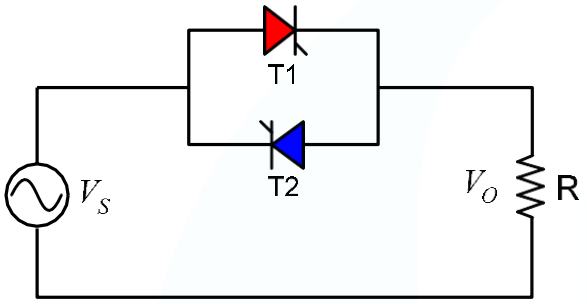
Current source inverters

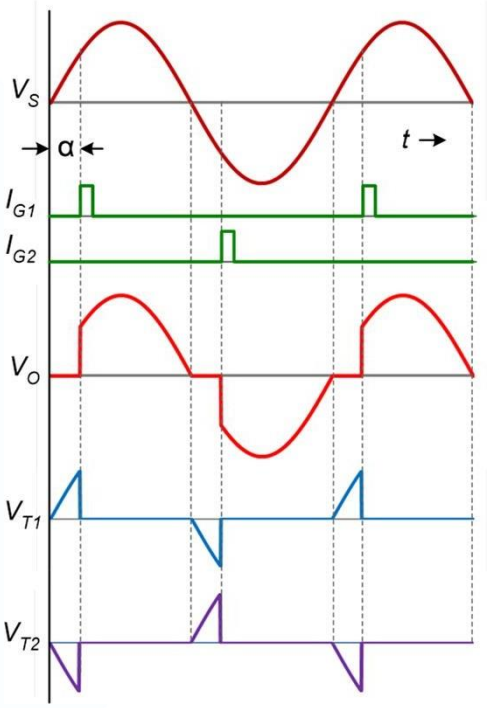
- The states 7, 8, and 9 produce zero ac line currents.
- In this case, the dc link current freewheels through either the switches S1 and S4, switches S3 and S6, or switches S5 and S2.
- The remaining states (1 to 6 in Table 14.4) produce nonzero ac output line currents.
- In order to generate a given set of ac line current waveforms, the inverter must move from one state to another.
- Thus, the resulting line currents consist of discrete values of current, which are i_i, 0, and -ii.
- The selection of the states in order to generate the given waveforms is done by the modulating technique that should ensure the use of only the valid states.

MODULE-5
AC Voltage Controllers

- Converts Fixed AC Voltage to Variable AC Voltage
- Thyristor based controller
- Two Types of Control
  - Phase Control
    - Conduction take place in a portion of each half cycle, starting from a specific phase angle (firing angle)
  - Integral Cycle Control
    - Conduction takes place for integral number of full cycles and turn off for further number of cycles.
    - Used in systems with large time constant

Basic Controller with R Load





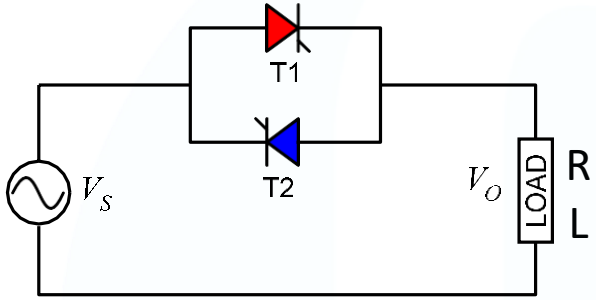
$$V_{O(RMS)} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi} V_m{}^2 \sin^2 \omega t.\, d\omega t\right]^{\frac{1}{2}} = \left[\frac{V_m{}^2}{2\pi}\left|\omega t - \frac{\sin 2\omega t}{2}\right|_{\alpha}^{\pi}\right]^{\frac{1}{2}}$$

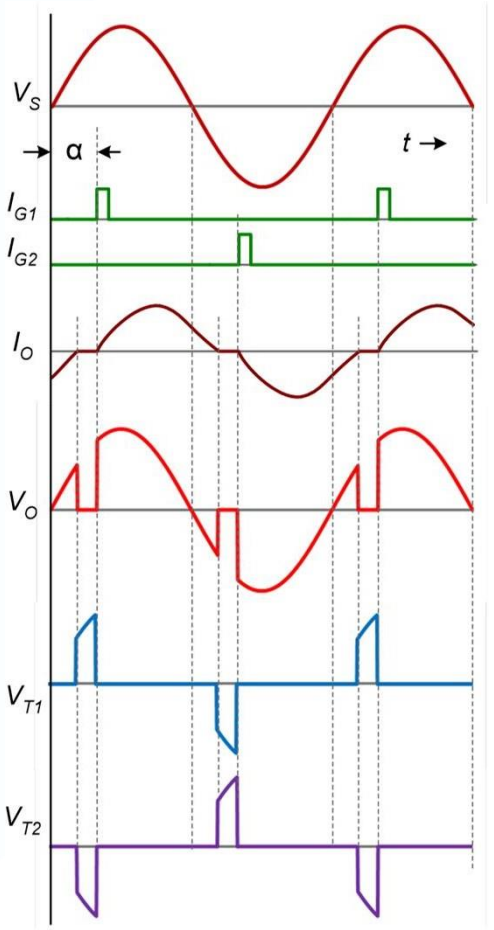
$$= \frac{V_m}{\sqrt{2}}\left[\frac{1}{\pi}\left((\pi-\alpha)+\frac{\sin 2\alpha}{2}\right)\right]^{\frac{1}{2}}$$

$$I_{O(RMS)} = \frac{V_{O(RMS)}}{R}$$

$$Input\ PF = \frac{Output\ Power}{Input\ VA} = \frac{P_O}{V_S \times I_O}$$

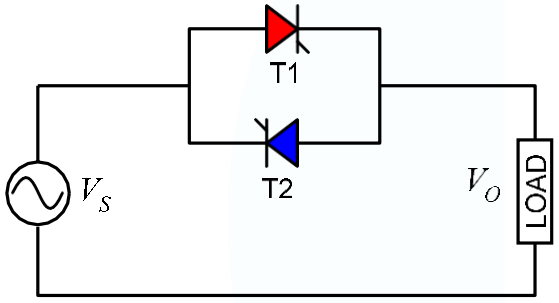
Basic Controller with RL Load





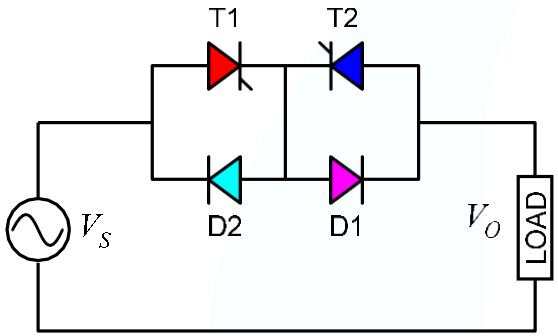
- Output current extends beyond the zero crossing point of input voltage
- Output voltage follows input as long as current is present
- Control may not be possible with highly inductive loads

Controller Types



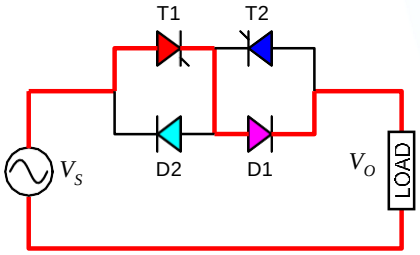
- Thyristors connected in antiparallel
- Each SCR conducts for one half cycle
- Cathodes are not connected to a common point; so isolated trigger circuit is needed
- Efficient, since only one SCR conducts during turn on

Controller Types

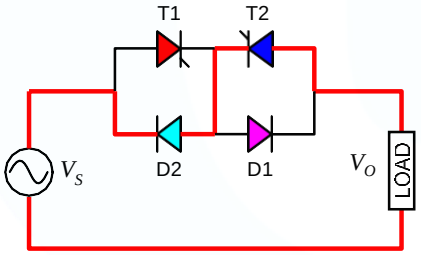


Cathodes of thyristors connected together; so isolated trigger circuit is not necessary

- Each SCR conducts for one half cycle along with a diode
- Less efficient, since one SCR and one diode conduct during turn on



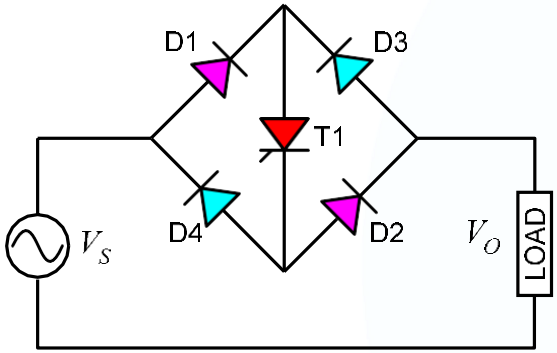
Conduction in Positive Half Cycle



Conduction in Negative Half Cycle

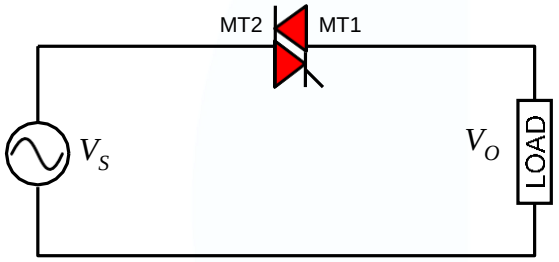
•

Controller Types



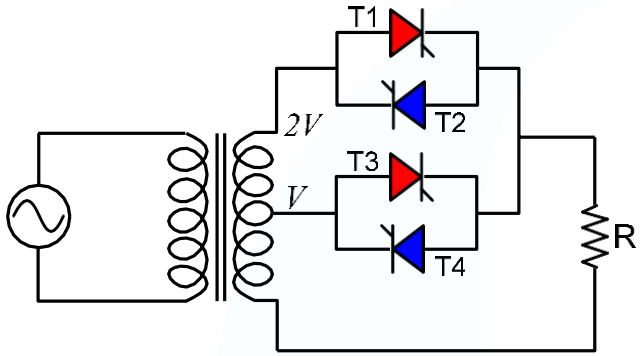
- Employs four diodes and one thyristor
- Less expensive
- Since there is only one thyristor, isolated trigger circuit is not necessary
- Low efficiency since one SCR and two diodes conduct during turn on

Controller Types



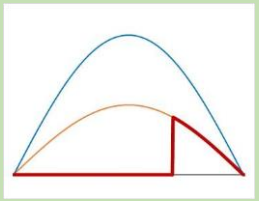
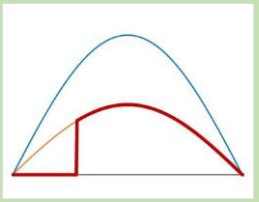
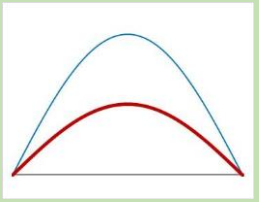
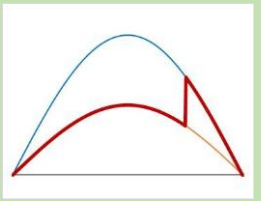
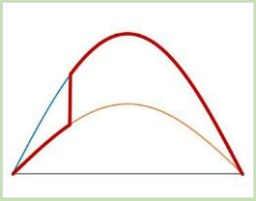
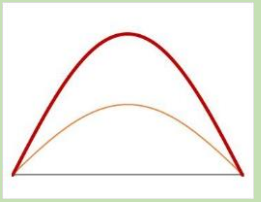
- Employs one triac only
- Suitable for low power applications
- Isolated trigger circuit is not necessary

Sequence control of AC Voltage



- May be of two stage or more
- Can work with resistive or inductive load
- Reduces waveform distortion in current for full range of control
- Improves average input power factor

Voltage Variation from 0 to V	Voltage Variation from V to 2V
T1, T2 **Off** T3, T4 controlled	T3, T4 **On** T1, T2 controlled

6 Module

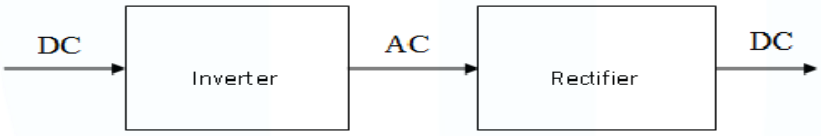
DC-DC converters–stepdown and step up choppers–single-quadrant, two-quadrant& four quadrant chopper–pulse width modulation &current limit control in dc-dc converters.Switchingregulators–buck,boost&buck-boost-continuousconductionmodeonly–waveforms–designoffilterinductance&capacitance

DC-DC converter (Chopper)

- Many industrial applications require power from dc voltage source
- E.g.:subwaycars, trolleybuses ,batteryoperatedvehicles, batterychargingetc…
- The*conversionoffixeddcvoltagetoanadjustabledcoutputvoltage*throughtheuseofsemiconductor devices can be carried out by the use of two types dc to dc converter given below
    - AC link chopper
    - DC chopper

AC linkchopper: **Dc** first converted to ac by using an inverter

- Dc first converted to ac by using an inverter
- Ac is then stepped up or down by using a transformer
- Which is then converted back to dc by using a diode rectifier
- As the conversion is in two stages, dc to ac and then ac to dc, ac link chopper is costly, bulky and less efficient

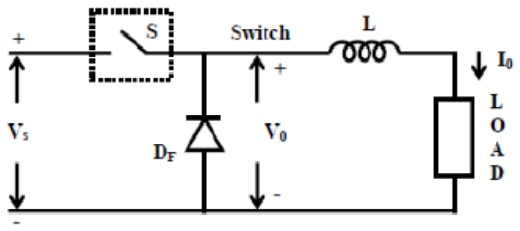


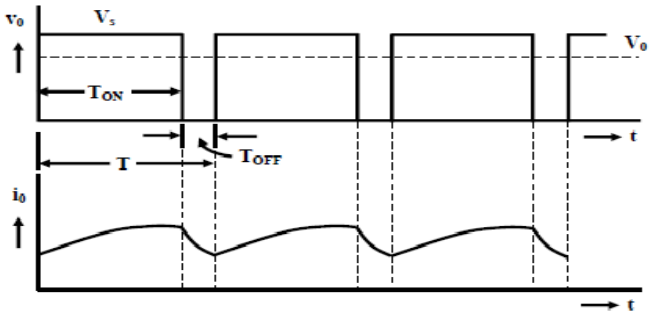
DC chopper

- *Chopper is a static device that convert fixed dc input voltage to a variable dc output voltage*
- Dc equivalent of an ac transformer
- Involves one stage conversion – more efficient

Step-down chopper

- A chopper is a high speed on/off semiconductor switch
- It connect source to load and disconnect the load from source at a fast speed
- Chopper is represented by a switch SW inside a dotted rectangle





- During the period Ton, chopper is on and load voltage is equal to source voltage Vs
- During the interval Toff, chopper is off, load current flows through the freewheeling diode FD
- As a result load terminal are short circuited by the FD and load voltage is therefore zero during Toff
- In this manner a chopped dc voltage is produced at the load terminal
- During Ton, load current rises whereas during Toff, load current decays

$$V_o = \frac{T_{on}}{T_{on} + T_{off}} V_s = \frac{T_{on}}{T} V = \alpha V_s$$

- Ton = on-time; Toff = off-time
- T=Ton+Toff = Chopping period
- Duty cycle

$$\alpha = \frac{T_{on}}{T}$$

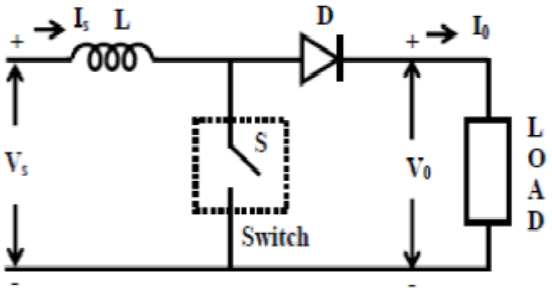
- Thus load voltage can be controlled by varying duty cycle

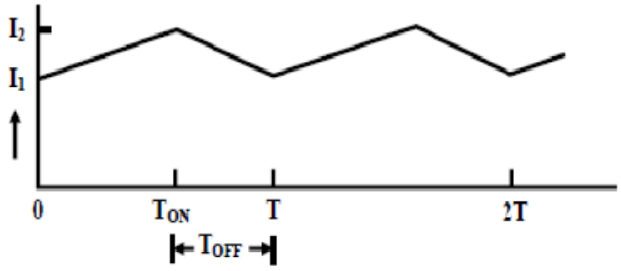
$$V_o = f \,.\, T_{on} \,.\, V_s$$

- Where f is the chopping frequency
- *Average output voltage is always less than the input voltage hence called as step down chopper*

Step–up chopper

- *Average output voltage greater than input voltage can obtained by using a chopper known as step-up chopper*
- A large inductor L in series with the source voltage is essential





- When chopper is on, inductor stores energy
- When chopper is off as the inductor current cannot die down instantaneously, this current is forced to flow through the diode and load for a time Toff
- As the current tends to decrease polarity of the emf induced in the L is reversed
- As a result voltage across the load become

$$V_o = V_s + L\frac{di}{dt}$$

exceeds the source voltage

- In this manner circuit act as a step up chopper
- Assuming linear variation of output current the energy input to inductor from the source during Ton is

$$W_{in} = (voltage\ across\ L)(average\ current\ through\ L)T_{on}$$

$$= V_s.\left(\frac{I_1 + I_2}{2}\right)T_{on}$$

- During Toff, when chopper is off, the energy released by the inductor to the load is

$$W_{off} = (voltage\ across\ L)(average\ current\ through\ L)T_{off}$$

$$= (V_o - V_s).\left(\frac{I_1 + I_2}{2}\right)T_{off}$$

- Considering the system to be lossless, these two energies will be equal

$$V_s\left(\frac{I_1+I_2}{2}\right)T_{on} = (V_o - V_s)\left(\frac{I_1+I_2}{2}\right)T_{off}$$

$$V_s.T_{on} = V_o.T_{off} - V_s.T_{off}$$

$$V_o.T_{off} = V_s(T_{on}+T_{off}) = V_s.T$$

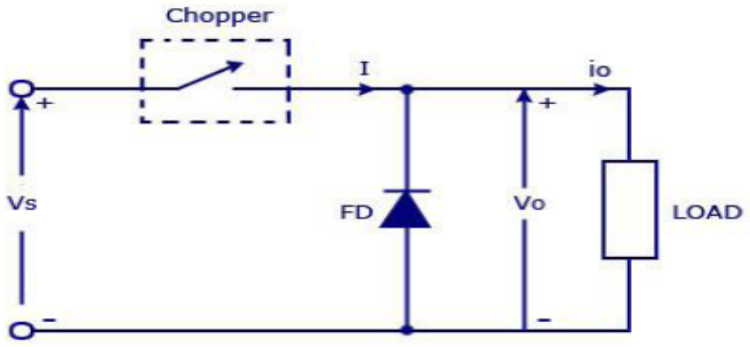
$$V_o = V_s\frac{T}{T_{off}} = V_s\frac{T}{T-T_{on}} = V_s\frac{1}{1-\alpha}$$

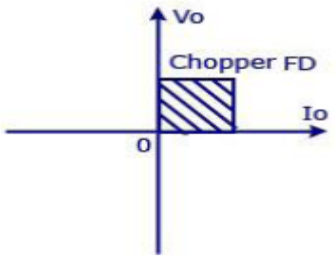
Types of chopper circuit

- Power semiconductor devices used in chopper circuit are unidirectional devices
- Polarities of output voltage and direction of output current is therefore restricted
- A chopper can however operate in any of the four quadrant, by an appropriate arrangements of the semiconductor devices
- This characteristics of their operation in any of the four quadrant form the basis of their classification as type-A, type-B etc... or class A, class B etc...

First quadrant or Type-A Chopper

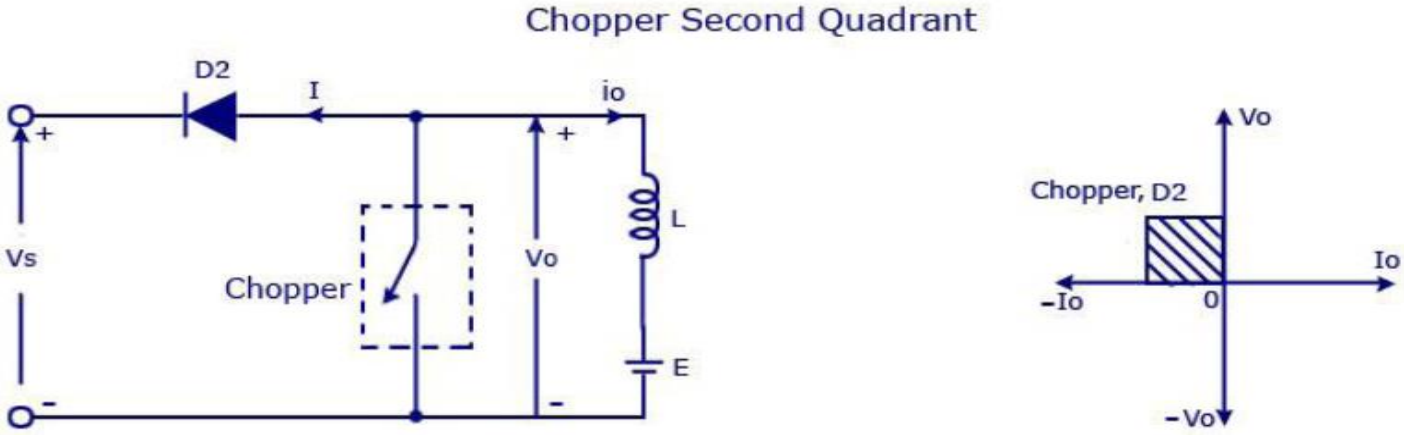
Chopper First Quadrant





- When chopper CH1 is on, Vo=Vs and current io flows in the direction as shown
- When CH1 is off, Vo=0, but io in the load continues to flowing in the same direction through freewheeling diode FD
- It is thus seen that average value of both load voltage and current are always +ve
- The power flow is always from source to load
- This chopper is also called step down chopper

Second quadrant or Type-B Chopper

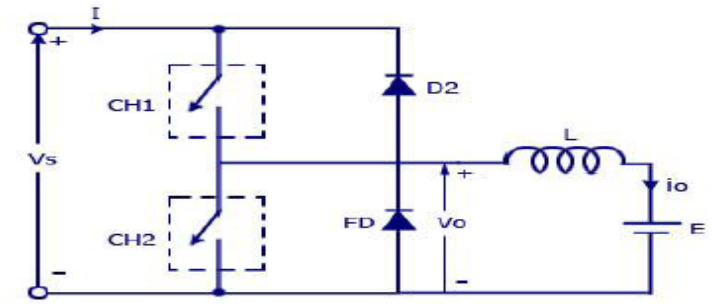


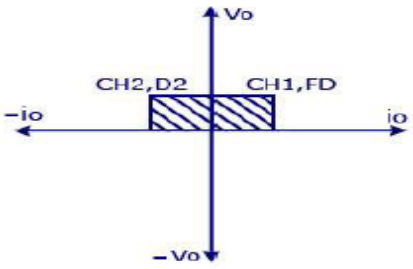
- Load must contain a dc source like a battery in this chopper
- When CH2 is on, vo=0 but load voltage E drives current through L and CH2
- Inductance L store energy during Ton of CH2
- When CH2 is off, vo=E+L(di/dt), exceeds source voltage Vs
- As a result diode D2 is forward biased and begins conduction, thus allowing power to flow to the source
- Chopper CH2 may be on or off, current Io flows out of the load, current Io is therefore treated as –ve
- Since Vo is always +ve and Io is –ve power flow is from load to source
- As load voltage Vo = E+L(di/dt) is more than source voltage Vs, type B chopper is known as step-up chopper

Two-quadrant type-A or Type–C

- Obtained by connecting Type-A and Type-B in parallel
- Output voltage Vo is always +ve because of the presence of freewheeling diode FD across the load
- When CH2 is on, or freewheeling diode FD conducts output voltage Vo=0

Chopper Two Quadrant





- When CH2 is on or diode D2 conducts, output voltage Vo=Vs
- The load current Io can however reverse its direction
- Load current is +ve when CH1 is on or FD conducts
- Load current is –ve when CH2 is on or D2 conducts
- In other words, CH1 and FD operate together as type-A chopper in first quadrant
- CH2 and D2 operate together as type-B chopper in second quadrant
- Average load voltage is always +ve, but average load current can be +ve or –ve
- This type of chopper operation is used for motoring and regenerative braking of dc motors

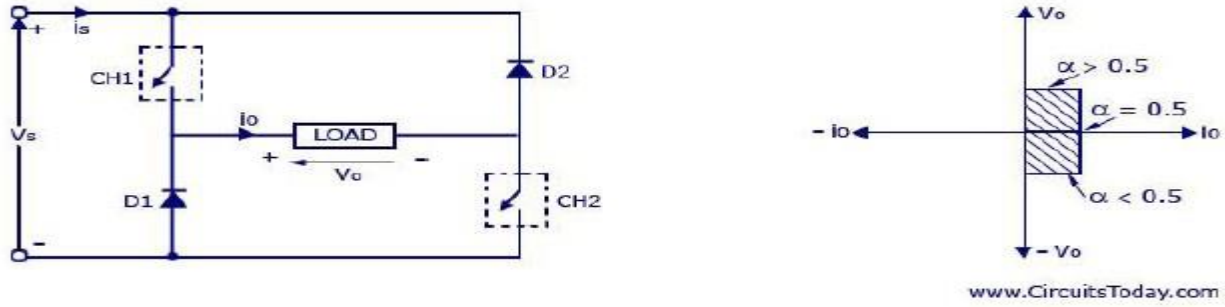
In short

This type of chopper is obtained by connecting type-*A* and type-*B* choppers in parallel as shown in Fig. 7.8 (*a*). The output voltage V_0 is always positive because of the presence of freewheeling diode FD across the load. When chopper CH2 is on, or freewheeling diode FD conducts, output voltage $v_0 = 0$ and in case chopper CH1 is on or diode D2 conducts, output voltage $v_0 = V_s$. The load current i_0 can, however, reverse its direction. Current i_0 flows in the arrow direction marked in Fig. 7.8 (*a*), *i.e.* load current is positive when CH1 is on or FD conducts. Load current is negative if CH2 is on or D2 conducts. In other words, CH1 and FD operate together as type-*A* chopper in first quadrant. Likewise, CH2 and D2 operate together as type-*B* chopper in second quadrant.

Average load voltage is always positive but average load current may be positive or negative as explained above. Therefore, power flow may be from source to load (first-quadrant operation) or from load to source (second-quadrant operation). Choppers CH1 and CH2 should not be on simultaneously as this would lead to a direct short circuit on the supply lines. This type of chopper configuration is used for motoring and regenerative braking of dc motors. The operating region of this type of chopper is shown in Fig. 7.8 (*b*) by hatched area in first and second quadrants.

Two-quadrant Type-B or Type-D

Two Quadrant Type B-chopper or D-chopper Circuit



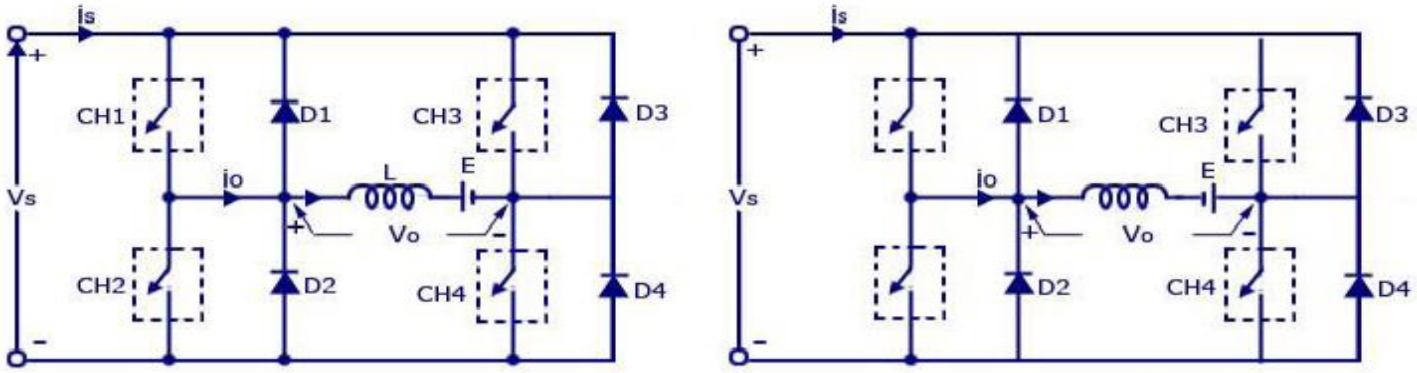
www.CircuitsToday.com

- Ton>Toff, α>0.5, Vo is +ve
- Ton<Toff, α<0.5, Vo is –ve
- Ton=Toff, α=0, Vo=0

- The out put voltage Vo=Vs when both CH1 and CH2 are on
- And Vo=-Vs, when both choppers are off but both diodes D1 and D2 conducts
- Average output voltage Vo is +ve when chopper turn on time is more than their turn off time
- The direction of load current is always +ve, because choppers and diodes can conduct current only in one direction
- As average values of both Vo and Io are +ve, chopper operation in first quadrant is obtained

Four quadrant chopper, Type-E

E-type Chopper Circuit Diagram With Load emf E and E Reversed



- Consist of four semiconductor switches, CH1toCH4 and four diodes from D1 to D4 in anti-parallel
- Numbering of chopper is corresponds to their respective quadrant of operation

First quadrant:

- CH4 is kept on, CH3 is kept off and Ch1 is operated
- With CH1 and CH4 on, load voltage Vo=Vs and load current begins to flow
- Vo and Io are +ve giving first quadrant operation
- CH1 is off, +ve current freewheels through CH4, D2

Second quadrant:

- CH2 is operated, CH1, CH3 and CH4 are kept off
- With CH2 on, reverse current flows through L, CH2, D4 and E
- Inductance L stores energy during the time CH2 on
- When CH2 is turned off, current is fed back to source through D1, D4
- Vo is +ve but Io is –ve, second quadrant operation of chopper
- For second quadrant operation load must contain emf E

Third quadrant:

- CH1 is kept off, CH2 is kept on and CH3 is operated
- Polarity of load emf must be reversed for this quadrant of operation
- When CH3 is on, load gets connected to source Vs so that both Vo and Io are –ve leading to 3rd quadrant of operation
- When CH3 is turned off, -ve current freewheels through CH2, D4

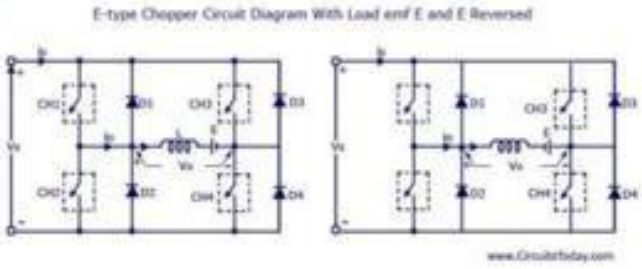
Fourth quadrant:

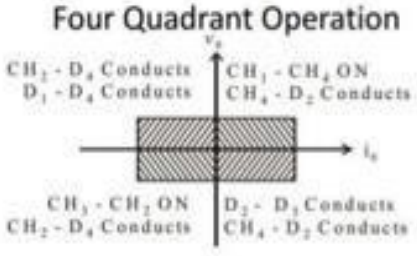
- CH4 is operated and other devices are kept off
- With CH4 on, +ve current flows through CH4, D2, L and E

FOUR QUADRANT CHOPPER, TYPE-E

- Inductance L stores energy during the time CH4 is on
- When CH4 is turned off, current is fed back to source through diodes D2, D3
- Load voltage is –ve but load current is +ve

Type-E chopper or the Fourth-Quadrant Chopper





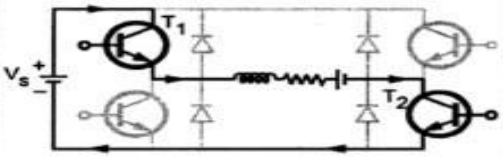
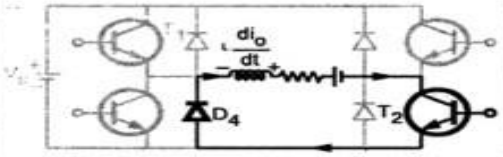
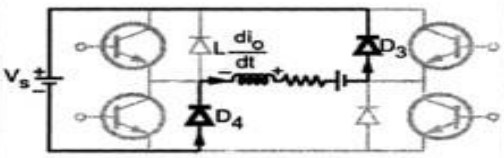
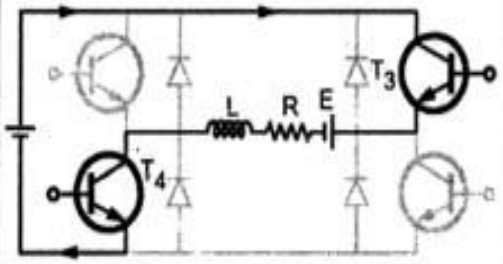
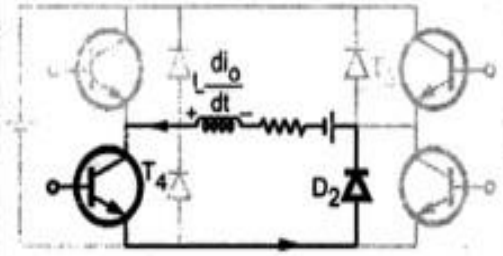
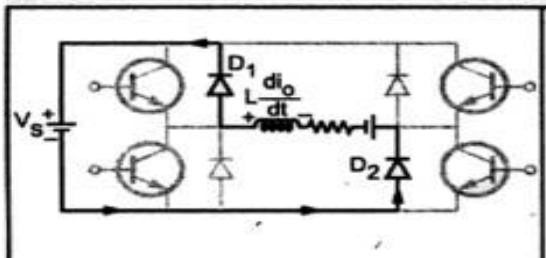
Equivalent circuit	Quadrant	Description
	I Forward motoring or rectifying.	T_1 and T_2 conducts load consumes the power from the source.
	I Forward motoring.	T_1 turned off but T_2 conducts Hence current i_o flows through T_2 and D_4. Load inductor induces voltage as shown freewheeling action takes place.
	IV Inverting operation i_o positive v_o negative.	T_2 is turned off. Hence inductance forces current through D_3 and D_4. This current flows through supply. load energy is fed to the supply.
	III Rectifying operation motor rotates in opposite direction.	To reverse the direction of rotation of the motor, T_3 and T_4 are turned on. v_o and i_o both are negative. E is shown negative since motor rotates in opposite direction.
	III Freewheeling operation motor rotates in the same direction.	T_3 is turned off, but T_4 remains on. To maintain the current in the same direction inductance generates voltage and i_o flows in same direction through D_2 and T_4 This is freewheeling action.
	II Inverting operation i_o negative v_o positive.	T_4 is turned off. Hence inductance forces current through D_1 and D_2. This current flows through supply. load energy is fed to the supply.

Table 4.5.3 Operation of four quadrant chopper

Four quadrant chopper has the capability to operate in all the four quadrants. Hence it is used in reversible dc drives. The braking is regenerative. Hence four quadrant chopper drives are highly efficient. Their dynamic response is also fast.

Control strategies

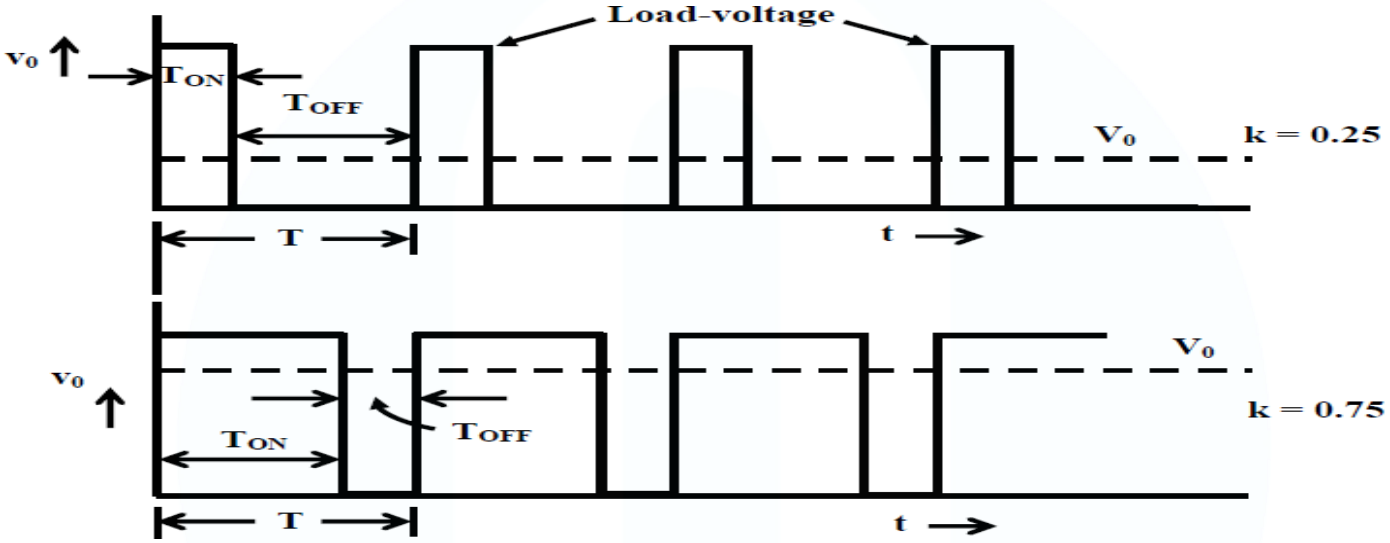
- The average value of the output voltagecan be varied by opening and closing the semiconductor switch
- The two types of control strategies (schemes) are employed in all cases. These are:
  (a) Time-ratio control, and
  (b)Current limit control

Time-ratio Control

- In the time ratio control the value of the duty ratio, TON/T=k is varied.
- There are two ways, which are constant frequency operation, and variable frequency operation.

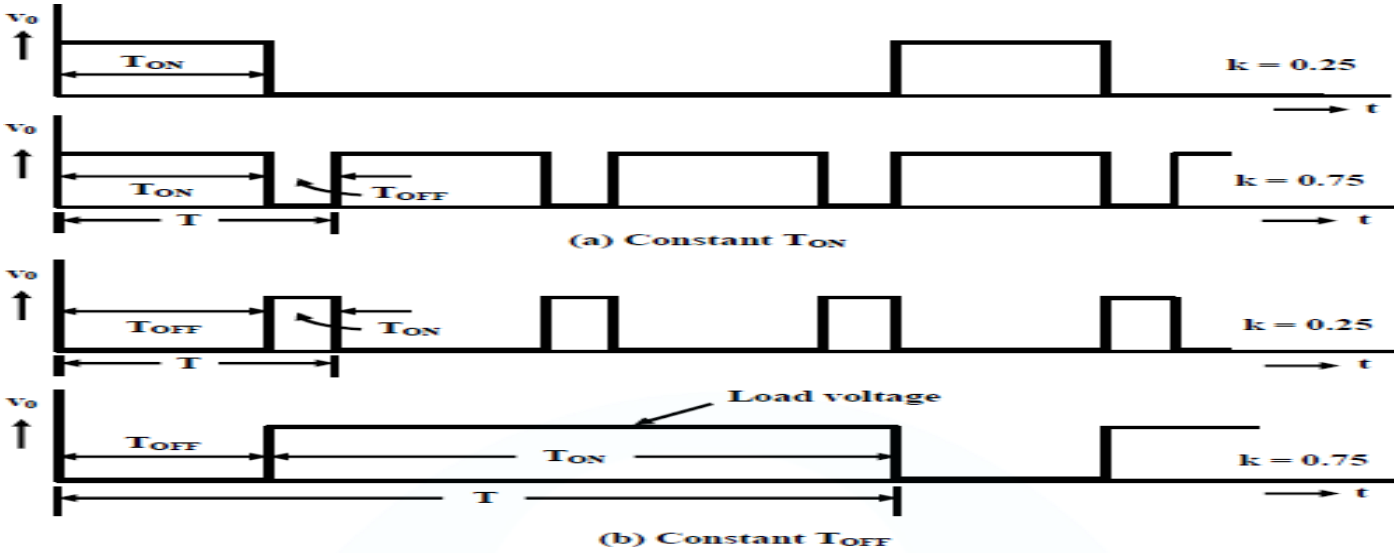
Constant Frequency Operation

- In this control strategy, the ON time, is varied, keeping the frequency (f=1/T), or time period T is constant.
- This is also called as *pulse width modulation control (PWM).*



Variable Frequency Operation

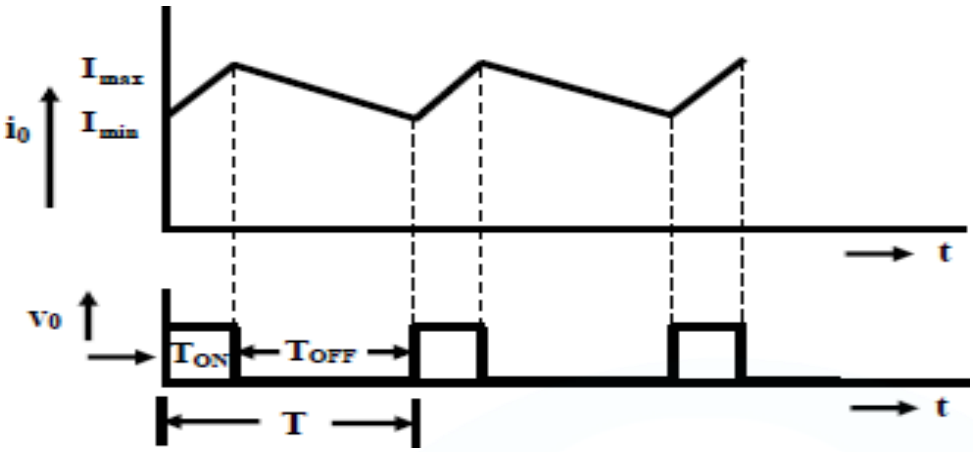
- In this control strategy, the frequency (f=1/T), or time periodT is varied, keeping either
- (a) the ON time, constant, or
- (b) the OFF time, constant.
- This is also called as frequency modulation control.
- Two cases with (a) the ON time, constant, and (b) the OFF time, constant, with variable frequency or time period are shown in Fig.
- The output voltage can be varied in both cases, with the change in duty ratio,Ton/T



- There are major disadvantages in this control strategy. These are:
  - The frequency has to be varied over a wide range for the control of output voltage in frequency modulation. Filter design for such wide frequency variation is, therefore, quite difficult.
  - For the control of a duty ratio, frequency variation would be wide. As such, there is a possibly of interference with systems using certain frequencies, such as signaling and telephone line, in frequency modulation technique.
  - The large OFF time in frequency modulation technique, may make the load current discontinuous, which is undesirable.
  - Thus, the constant frequency system using PWM is the preferred scheme for dc-dc converters (choppers).

Current-limit control

- As can be observed from the current waveforms for the types of dc-dc converters described earlier, the current changes between the maximum and minimum values, if it (current) is continuous.
- In the current limit control strategy, the switch in dc-dc converter (chopper) is turned ON and OFF, so that the current is maintained between two (upper and lower) limits..When the current exceed upper (maximum) limit, the switch is turned OFF
- During OFF period, the current freewheels in say, buck converter (dc- dc) through the diode, DF, and decreases exponentially.
- When it reaches lower (minimum) limit, the switch is turned ON.
- This type of control is possible, either with constant frequency, or constant ON time
- This is used only, when the load has energy storageelements, i.e. inductance, L.
- The reference values are load current or load voltage.
- In this case, the current is continuous, varying between Imax and Imin , which decides the frequency used for switching.
- The ripple in the load current can be reduced, if the difference between the upper and lower limits is reduced, thereby making it minimum.
- This in turn increases the frequency, therebyincreasing the switching losses.



Switching regulators

- DC converters can be used as switching mode regulators to convert a dc voltage, normally unregulated to a regulated dc voltage
- The regulation is normally achieved by PWM at a fixed frequency and the switching device is normally BJT, MOSFET or IGBT
- The ripple content is normally reduced by an LC filter
- There are four basic topologies of switching regulators

  Buck regulator

  Boost regulator

  Buck-boost regulator

  Cuk regulator

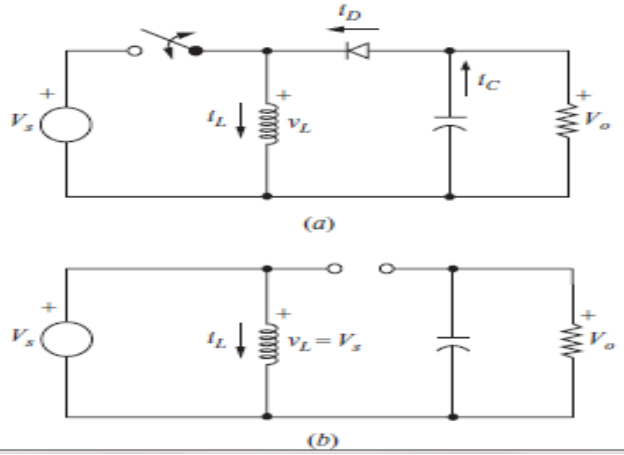
6.6 THE BUCK-BOOST CONVERTER

Another basic switched-mode converter is the buck-boost converter shown in Fig. 6-11. The output voltage of the buck-boost converter can be either higher or lower than the input voltage.

Voltage and Current Relationships

Assumptions made about the operation of the converter are as follows:

1. The circuit is operating in the steady state.
2. The inductor current is continuous.
3. The capacitor is large enough to assume a constant output voltage.
4. The switch is closed for time DT and open for $(1-D)T$.
5. The components are ideal.



Analysis for the Switch Closed When the switch is closed, the voltage across the inductor is

$$v_L = V_s = L\frac{di_L}{dt}$$

$$\frac{di_L}{dt} = \frac{V_s}{L}$$

The rate of change of inductor current is a constant, indicating a linearly increasing inductor current. The preceding equation can be expressed as

$$\frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{DT} = \frac{V_s}{L}$$

Solving for Δi_L when the switch is closed gives

$$(\Delta i_L)_{\text{closed}} = \frac{V_s DT}{L} \tag{6-45}$$

Analysis for the Switch Open When the switch is open, the current in the inductor cannot change instantaneously, resulting in a forward-biased diode and current into the resistor and capacitor. In this condition, the voltage across the inductor is

$$v_L = V_o = L\frac{di_L}{dt}$$

$$\frac{di_L}{dt} = \frac{V_o}{L}$$

Again, the rate of change of inductor current is constant, and the change in current is

$$\frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{(1-D)T} = \frac{V_o}{L}$$

Solving for Δi_L,

$$(\Delta i_L)_{\text{open}} = \frac{V_o(1-D)T}{L} \tag{6-46}$$

Again, the rate of change of inductor current is constant, and the change in current is

$$\frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{(1-D)T} = \frac{V_o}{L}$$

Solving for Δi_L,

$$(\Delta i_L)_{\text{open}} = \frac{V_o(1-D)T}{L} \tag{6-46}$$

For steady-state operation, the net change in inductor current must be zero over one period. Using Eqs. (6-45) and (6-46),

$$(\Delta i_L)_{\text{closed}} + (\Delta i_L)_{\text{open}} = 0$$

$$\frac{V_s DT}{L} + \frac{V_o(1-D)T}{L} = 0$$

Solving for V_o,

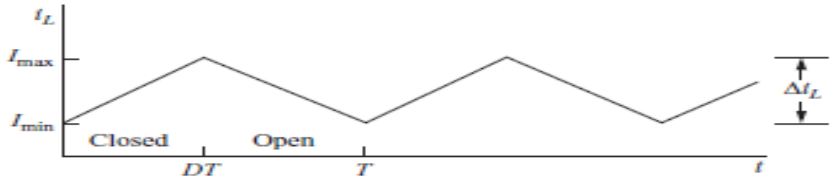
$$\boxed{V_o = -V_s\left(\frac{D}{1-D}\right)} \tag{6-47}$$

INDUCTOR CURRENT , DESIGN OF FILTER INDUCTANCE OR CRITICAL INDUCTANCE

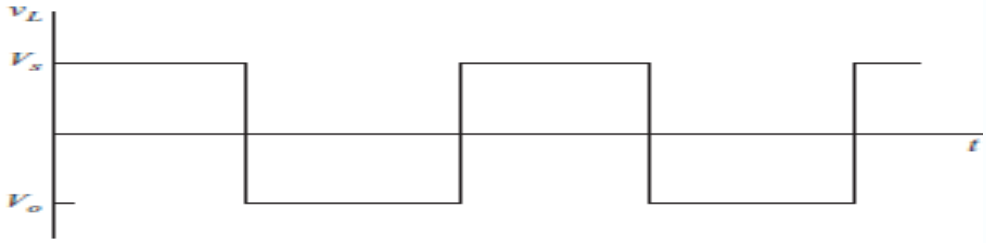
source voltage. *Output voltage magnitude of the buck-boost converter can be less than that of the source or greater than the source, depending on the duty ratio of the switch.* If $D > 0.5$, the output voltage is larger than the input; and if $D < 0.5$, the output is smaller than the input. Therefore, this circuit combines the capabilities of the buck and boost converters. Polarity reversal on the output may be a disadvantage in some applications, however. Voltage and current waveforms are shown in Fig. 6-12.

Note that the source is never connected directly to the load in the buck-boost converter. Energy is stored in the inductor when the switch is closed and transferred to the load when the switch is open. Hence, the buck-boost converter is also referred to as an *indirect* converter.

Power absorbed by the load must be the same as that supplied by the source, where

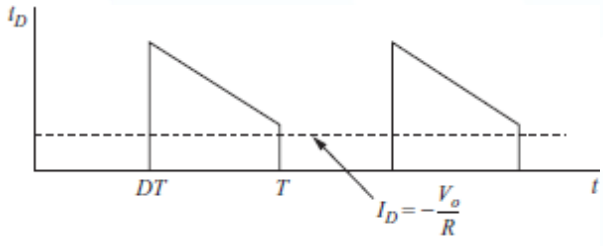


(*a*)

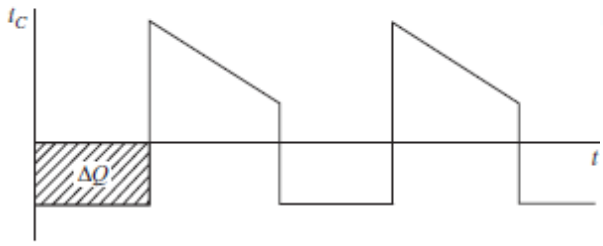


(*b*)

Figure 6–12 Buck-boost converter waveforms. (*a*) Inductor current; (*b*) Inductor voltage; (*c*) Diode current; (*d*) Capacitor current.



(*c*)



(*d*)

Figure 6-12 *(continued)*

Figure 6-12 *(continued)*

$$P_o = \frac{V_o^2}{R}$$

$$P_s = V_s I_s$$

$$\frac{V_o^2}{R} = V_s I_s$$

Average source current is related to average inductor current by

$$I_s = I_L D$$

resulting in

$$\frac{V_o^2}{R} = V_s I_L D$$

Substituting for V_o using Eq. (6-47) and solving for I_L, we find

$$I_L = \frac{V_o^2}{V_s R D} = \frac{P_o}{V_s D} = \frac{V_s D}{R(1-D)^2} \tag{6-49}$$

Maximum and minimum inductor currents are determined using Eqs. (6-45) and (6-49).

$$I_{\max} = I_L + \frac{\Delta i_L}{2} = \frac{V_s D}{R(1-D)^2} + \frac{V_s DT}{2L} \tag{6-50}$$

$$I_{\min} = I_L - \frac{\Delta i_L}{2} = \frac{V_s D}{R(1-D)^2} - \frac{V_s DT}{2L} \tag{6-51}$$

$$(Lf)_{\min} = \frac{(1-D)^2 R}{2} \tag{6-}$$

or

$$\boxed{L_{\min} = \frac{(1-D)^2 R}{2f}} \tag{6-}$$

where f is the switching frequency.

Output Voltage Ripple

The output voltage ripple for the buck-boost converter is computed from capacitor current waveform of Fig. 6-12*d*.

$$|\Delta Q| = \left(\frac{V_o}{R}\right) DT = C \Delta V_o$$

Solving for ΔV_o,

$$\Delta V_o = \frac{V_o DT}{RC} = \frac{V_o D}{RCf}$$

or

$$\boxed{\frac{\Delta V_o}{V_o} = \frac{D}{RCf}} \tag{6-}$$

Refer your class notes for buck and boost regulator derivation