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Bonding techniques for MEMS

Bonding is one of the essential technologies for MEMS andMicrosystems packaging. It is required in the following three principal areas:

1. Joining one substrate to another substrate such as wafer towafer or wafer to other supporting wafers made of glass, quartz, sapphire, ceramic and metals.
2. Securing micro components to support substrates such asmounting silicon dies to their constraint bases made ofglass or ceramic
3. Attaching wires and electrical leads to and from transducers in micro devices

Types (1) and (2) relate to the **"surface bonding"**,whereas Type (3) is referred to as **"wire bonding"**. Two principal requirements for achieving good surfacebonding for micro components are (1) intimate surface contact, and (2) temperature. "Intimate surface contact" isrequired for quality of the bonding and "temperature" supplies the required energy for the bonding. Intimate surface contact requires adequatecontact pressure as well as "clean" contact surfaces.

Surface bonding

There are four (4) techniquesavailable for surface bonding in MEMS and microsystems:

(1) Adhesives

(2) Eutectic soldering

(3) Anodic bonding

(4) Silicon fusion bonding (SFB)

Adhesives

This bonding technique has been in existence for decades.Many die attaches in integrated circuits are produced by thismethod. It is the least expensive way to bond two separatesurfaces. A generic arrangement of this bonding technique isillustrated in figure:

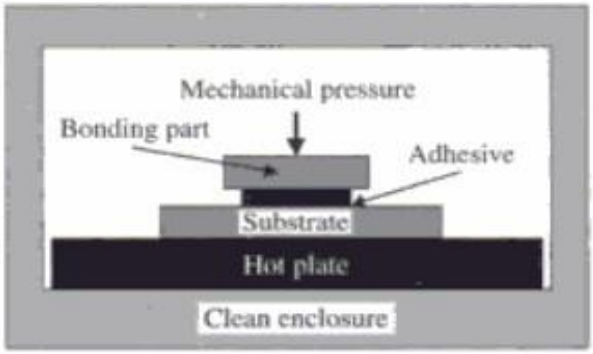


Fig: Bonding by adhesion

The chamber in which bonding takes place supplies therequired heating to the substrate for reaching the desiredbonding temperature. This temperature usually is close to butbelow the glass transition temperature, T_g, of the thin adhesivethat is dispensed on the top of the substrate by a micro dispenser. The part to be bonded is then placed on the top of theadhesive film. Mechanical pressure is normally applied toensure the quality of bonding. The chamber must bekeptclean, free from dust or other solid contaminant. Often thebonding operation is carried out in vacuum.

Epoxy resinand**silicone rubbers**are two commonly used adhesives. Epoxy resins provide flexibility for the bonded dies as well as good sealing. Good bonding rely on surface treatments and curing processcontrol. They are also vulnerable to thermal environment. The bond should be kept below T_g, which is normally 150 -170^{0}C.Soft silicone rubbersare used for bondingparts require " flexibility ."It is vulnerable to chemicals and air.

Eutectic soldering

Eutectic bonding involves the diffusion of atoms of eutecticalloys into the atomic structures of the materials to be bondedtogether, and thus forms solid bonding of these materials. A commonly used material to form a eutectic alloywith silicon is thin film made of gold (Au) or alloys thatinvolve gold.

Eutectic bonding takes place when the assembly of the twobonding surfaces, e.g. silicon substrate, with a eutectic alloycomponent such as gold is heated to the temperature above theeutectic temperature. A eutectic temperature is the lowestfusion temperature of an alloy with melting point lower thanthat of any other combination of the same components. Atsuch time, the atoms of the interface material, e.g,. Au, start todiffuse rapidly into the contacting substrates of silicon. Sufficient migration of these atoms into the bonding substratesurface will result in the formation of a eutectic alloy. EgAu-Si. As the temperature continues to rise above the eutectictemperature, more eutectic alloy is formed. This process willcontinue until the atoms, e.g,.the gold atoms, in the eutecticalloy at the interface material near complete depletion.Thenewly created eutectic alloy at the interface serves as a solidbond as well as hermetic sealing for many MEMS andmicrosystems applications.

A thin film alloy made of 80% Au-20% Snis sandwiched betweenthe silicon piezoresistor and the silicon substrate as in figure. The gold-tin alloy film was 0.025 mm thick. Aweight that was equivalent to 1 MPa was placed on the top ofthe upper silicon substrate to ensure intimate contact of thebonding surfaces and the thin gold-tin film during the bondingprocess. The assembly was placed in a clean evacuatedenclosed chamber in which heat was supplied. The chamberwas gradually heated to 280°C and held at that temperaturefor one hour. The chamber was then cooled to room temperature in three hours.As for bonding by adhesives, eutectic bonding requiresproper process control.

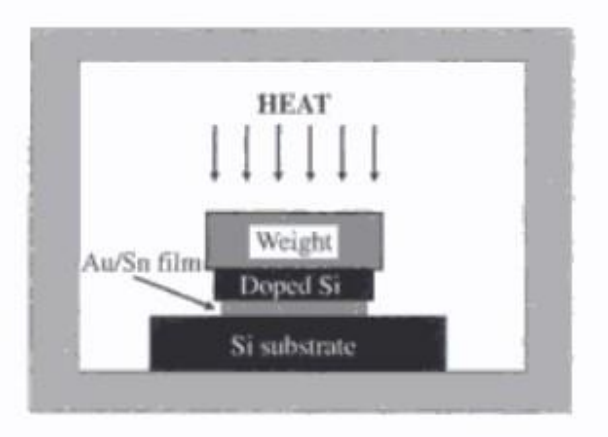


Fig: Eutetic bonding chamber

Anodic bonding

This bonding technique is most commonly used in bondingwafers of different materials. It is also called electrostaticbonding, or field-assisted thermal bonding.Anodic bonding is popular in microsystems packaging due tothe relatively simple set-up with inexpensive equipmentrequired. Anodic bonding providesreliable hermetic sealing that is important for applications inmicro valves and channels in microfluidics networks, as well asfor micro pressure sensor dies. Another major advantage ofthis bonding technique is that bonding can take place at low tomoderately high temperatures in the range 180 to 500^0Cwhich results in low risk of residual stress and strain in thematerials after the bonding.

Anodic bonding has been used to bond wafers made of thefollowing materials:

Glass-to-glass

Glass-to-silicon

Glass-to-silicon compounds, e.g. GaAs

Glass-to-metals

Silicon-to-silicon

However, the most common application of anodic bonding isto bond wafers made of Pyrex glass or quartz to silicon wafers.

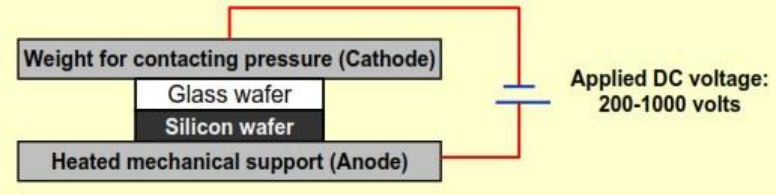


Fig: Anodic bonding of Silicon to glass

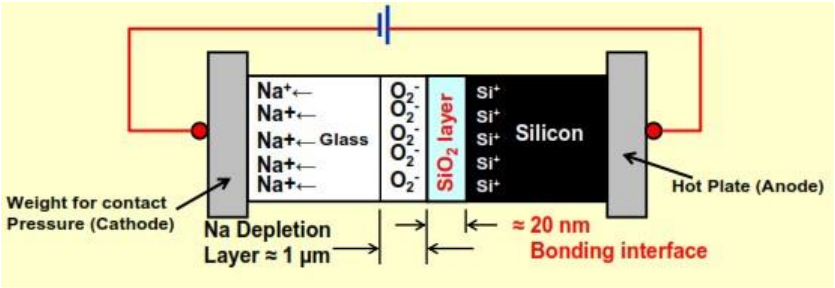


Fig: Formation of SiO_2 layer in anodic bonding

The set up for anodic bonding of a sodium rich wafer e.g, Pyrex 7740 glass (rich in sodium) to silicon wafer is shown in figure. A modest weight is normally placed on the top of the pyrex glass wafer to ensure good contacting pressure. An electric field with a 200-1000 DC voltage is applied to the system. The sandwiched delectricpyrex glass and silicon wafers between the two electrodes form an effective parallel plate capacitor. The bonding between them is accomplished by the formation of an extremely thin layer of SiO_2 interface as the result of the applied electric field. Under the influence of electric field, the sodium ions (Na^+) in the glass are attracted towards the negatively charged cathode, which leaves behind an Na^+ depletion zone with negatively charged O_2 ions. These O^-_2 ions can be chemically bonded to the contacting Si^+ions with the supplied heating of the system, and form a very thin layer of $SiO_2$of approximately 20nm at the interface. Anodic bonding normally takes 10 to 20 minutes to bond 100mm diameter silicon and glass wafers in an evacuated chamber at 450^0C with 1000 V DC. Successful anodic bonding requires the maintaining of constant temperture, applied voltage and current density conditions during the bonding process. The surfaces of the wafers must be flat and smooth.

Silicon fusion bonding (SFB)

SFB is an effective and reliable technique for bonding two silicon wafers or substrates without the use of intermediate adhesives. It is relatively simple and inexpensive bonding process. SFB has been used to bond

- Silicon-to-silicon
- Silicon with oxide-t o -silicon
- Silicon with oxide-t o silicon with oxide
- GaAs-to-silicon
- Quartz-to-silicon
- Silicon-to-glass

SFB is accomplished by the induced chemical forces at the interface and bonding is spontaneous at oxidising ambient, to be followed by annealing at high temperature.

SFB by hydration

This is a common process that is used in SFB. The procedureinvolved in this bonding process is first to introduce oxygen(O)-hydrogen (H) bonds, called the silanol bond, at the interface through a hydration process. Dehydration occurs whenthe wafers with silanol bonds at their surfaces are put intointimate contact, resulting in the formation of water (H_2O)vapour that escapes to the environment upon subsequentannealing at high temperature. What are left behind are theexcessive oxygen atoms that form a siloxane network at theinterface to form strong bonding of the two wafer surfaces.

The chemical reaction for this process is

(Si with OH) + (OH with Si) $\rightarrow$ H_2O + (Si-O-Si)

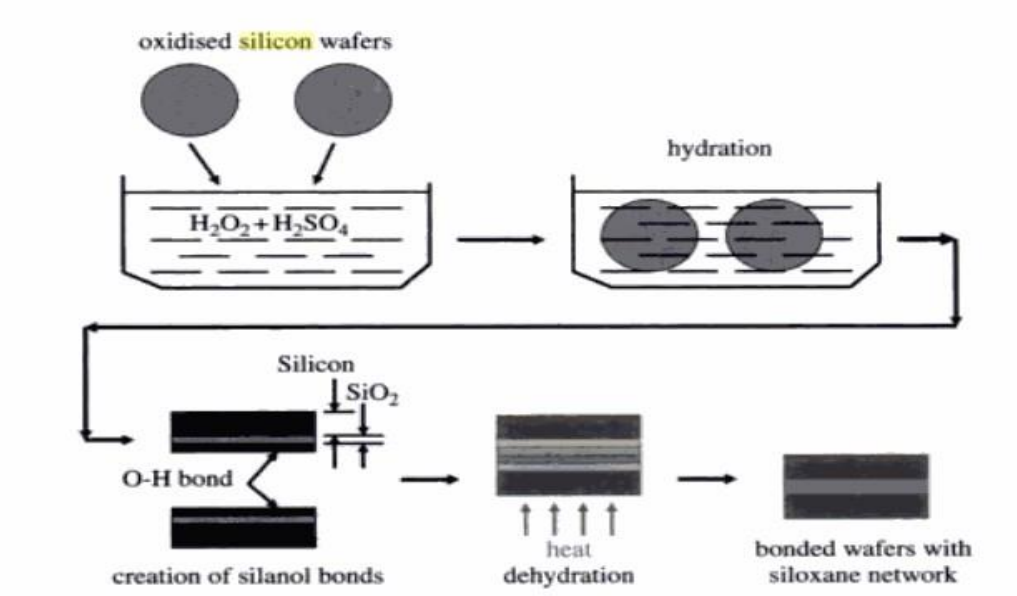


Fig: SFB by hydration

The two oxidisedsiliconwafers are soaked in the (H_2O_2-H_2SO_4) solvent in the hydration process. An O-H bond (silanol bond) will be developed ontheoxidised layer surface after the wafers are removed fromthe acid solution and rinsed with deionised water. The twowafers are then placed one on top of the other to form a bond. Heating the stacked wafers will drive the O2 and H2 molecules in the contacted O-H bond to form a Si-O-Si bond between the two wafers.

SFB by hydrophilic

Another popular SFB technique involves the use of a hydrophilic process. The wafers are soaked in boiling nitric acid tocreate the hydrophobic surfaces for bonding. Bonding of thetwo wafers takes place even at room temperature. However,an annealing process at high temperature is normally appliedto enhance the bonding. The bonding mechanism in hydrophilic is not the same as that in hydration. Hydrogen-inducedvan der Waals forces are believed to be the principal bondingforces for the wafers in the hydrophilic process.

Silicon-on-Insulator (SOI)

SOI is a process that is used in microelectronics to avoid leakage of charges in p-n junctions. It involves bonding the silicon with an amorphous material such as SiO_2. Silicon is a semiconductor which conducts electricity at high electric potentials or at elevated temperature. For example, siliconbecomes increasingly electrical conductive at a temperature above 125^0C. This transformation of silicon from a semiconductor to a conductor limitssilicon sense elements to being effective in elevated temperature applications. Theprocess of silicon-on-insulator offers a viable solution to this problem.

The process uses two silicon substrates, one with one of its surfaces heavily doped with boron atoms to produce a layer of p-silicon, and the other with a thin silicon oxide film on one of its faces, as shown in Figure (a). The two substrates are then mounted one on the topof the other as shown in Figure (b). The process of silicon fusion bonding joins thetwo substrates together. The bonded substrates are then exposed to etching to etch theexposed surfaces of the bonded substrates. The heavily p-doped region can act as an etch stop. Consequently, one may obtain either ap-silicon layer on the SiO_2 insulator, or sandwiched silicon substrates withSiO_2insulator in between as in Figure (c). This technique, which involves bonding of substrates followed by etching the bonded substrates is termed as bonding-and – etchback technique

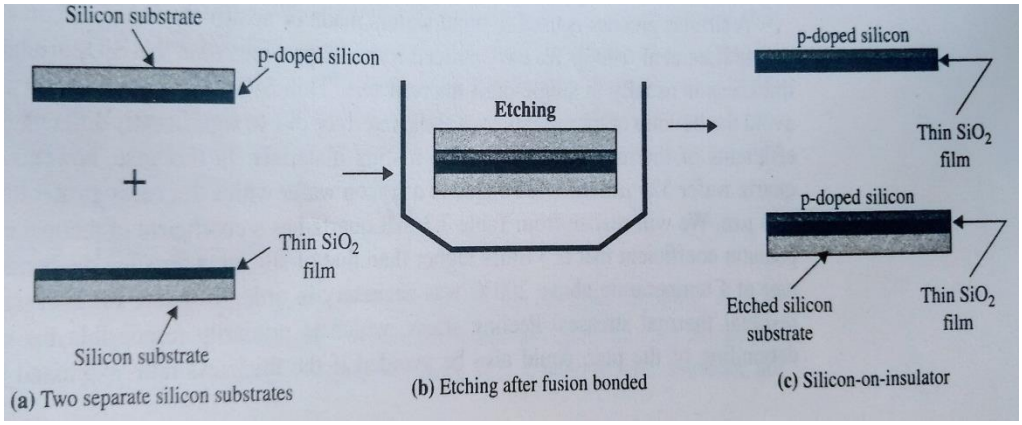


Fig: Silicon-on-insulator process

Wire bonding

Wire bonding provides electrical connection to or from the core elements. Common wire materials are gold and aluminum. Other wire materials include copper, silver, and palladium. Wiresizes are in the order of 20 to 80 μm in diameter. Three wire bonding techniques arecommonly used by the industry:

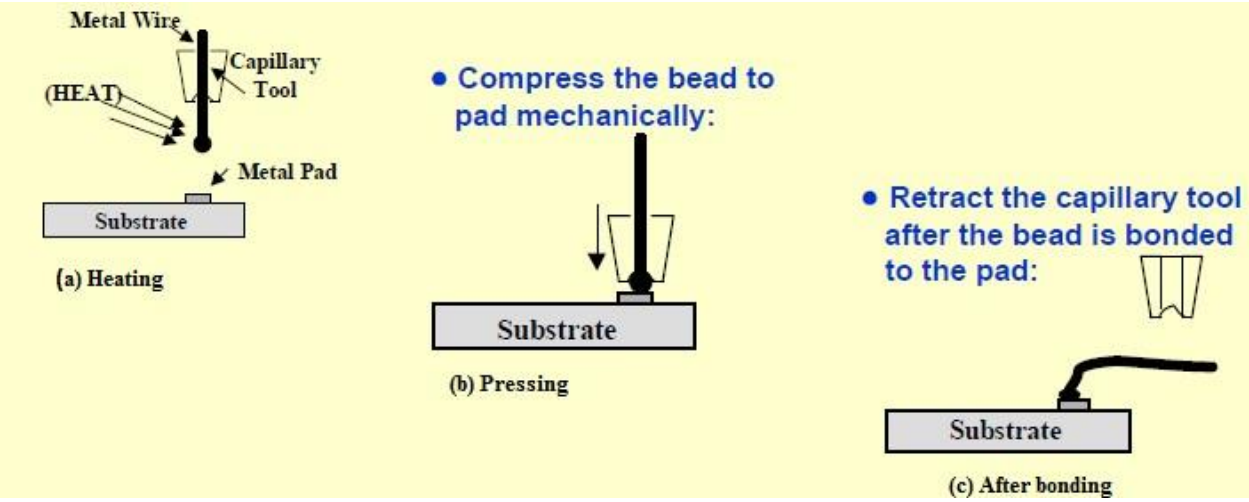
(1) thermocompression

(2) wedge-wedge ultrasonic wire bonding

(3) thermosonic

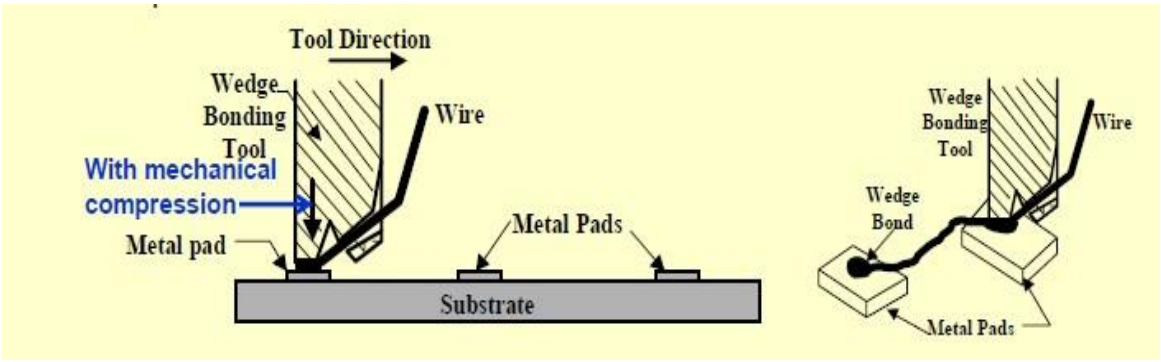
Thermocompression Wire Bonding

The principle of thermocompressionwire bonding is to press heated metal balls onto metal pads. In Figure (a), the metal wire is fed through a capillary bonding tool withthe tip of the wire above the metal pad. A torch heats the wire tip to about 400°C, atwhich temperature the wire tip tums into the shape of a ball. At this point, the tool which has a hemispherical mold shape at the end, is lowered to press the ball onto thepad (Fig. (b)). After typically 40 ms of pressing, the tool is retracted and the wireis bonded to the pad, as illustrated in Figure (c). The solid bonding of the wireball to the flat metal pad is accomplished by two physical actions: the plastic deformation of the ball onto the pad by the tool and the atomic interdiffusion of the twobonded materials.



Wedge-wedge Ultrasonic Bonding

Unlike thermocompressionbonding,ultrasonic wire bonding is a low-temperature process. The bonding tool is in theshape of a wedge, through which the wire is fed. The energy supplied for the bonding is an ultrasonic wave that is generated by a transducer that vibrates the tool ata frequency from 20 to 60 kHz. The bonding tool travels in parallel to the bondingpad as illustrated in Figure (a). After moving overtop the desired bonding pad, the wedge tool is lowered to the pad's surface. A compressive force is appliedand a burst of ultrasonic energy is released to break down the contact surfaces andachieve the desired surface bonding (Fig. (b)). Typical time required for bonding is about 20ms



Thermosonic Bonding

This technique combines the previous two wire bonding techniques. Ultrasonic energy is used with thermocompression at moderate temperatures of 100 to 150°C. A capillary tool is used to provide ball joints.For MEMS application, wire bonding is often combined with ball-wedge jointsor wedge-wedge joints as illustrated in figure below

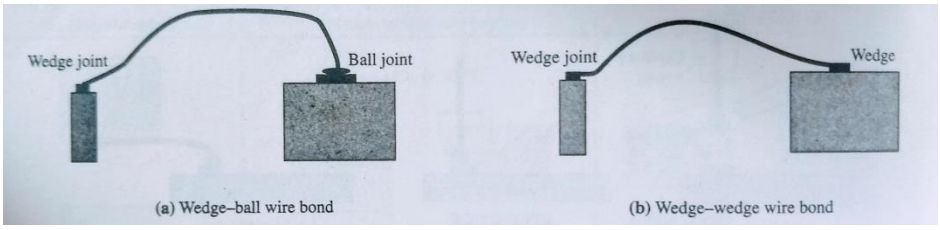


Fig: Wire bonding of microsystem

Sealing

Sealing is a key requirement in MEMS and microsystems packaging.Hermetic sealing is essential in devices or systems such as: microfluidic, optoMEMS, bioMEMS, pressure sensors, etc.Mechanical sealing of the interfaces of mating components by epoxy resin iscommon in microchannels in fluidic systems.Thismethod of sealing is usually adequate for systems that do not operate at elevatedtemperature and/or with toxic working media, and they are not expected to last for along period of time.

Sealing by Microshells

Microshells are produced to protect the delicate sensing or actuating elements in microdevices.Asurface micromachining technique is used to produce microshells. The procedure involves depositing a sacrificial layer over the die to be protected, as shown inFigure (a). A shell material is then deposited over the sacrificial layer. An etchingprocess then follows to remove the sacrificial layer. Consequently, a gap space between the die and the microshell is created as shown in Figure (b). These gapscan be as small as 100 nm

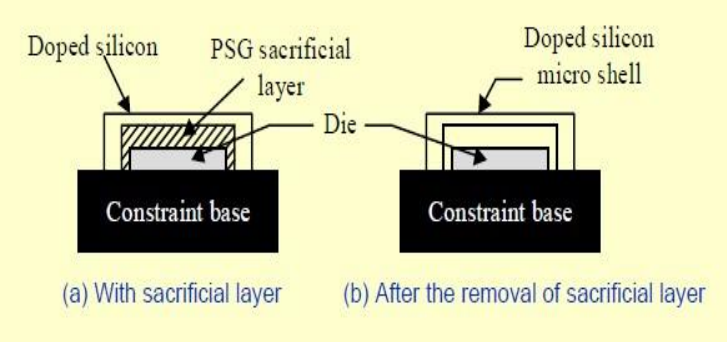


Fig: Sealing by microshell

Reactive Sealing Technique

This technique relies on specific chemical reactions to produce the necessary sealing of the mating components. As illustrated in figure the encapsulant cover for the die is initially placed on the top of the die/constraint base with small gaps (Fig (a)). The unit is subject to a chemical reaction such as the thermal oxidation process. The growth of SiO_2 from both ends of the silicon

encapsulant and the constraint base can provide a reliable and effective seal for the encapsulated die.

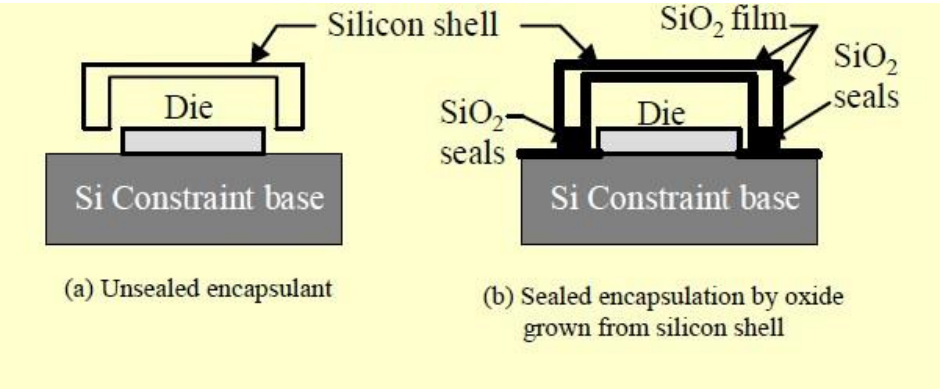


Fig: Reactive sealing

Assembly of microsystems

Assembly of microsystems with components whose sizes range from 1 µm to a few millimeters presents major challenges to engineers in terms of reliability and cost. Following are the reasons for the high cost associated with microassembly.

1. There is lack of standard procedures and rules for such assemblies. Products are assembled according to the specific procedures chosen on the basis of either individual customer requirements or the personal experience of the design engineer.
2. There is lack of effective tools for micro assembly. Tools such as microgrippers manipulators, and robots are still being developed. Microassemblies also require reliable visual and alignment equipment such as stereo electron microscopes and electron-beam, UV-stimulated beam, or ion beam imaging systems specially designed for microsystem assembly.
3. There is a lack of established methodology in setting proper tolerances of parts in insertion and assembly.
4. Microcomponents to be assembled are mostly made by physical-chemical processes that have strong material dependence. Traditional assembly techniques are not suitable for microdevices because of the minute size of the components and the close tolerances in the order of submicrometer. Moreover, chemical and electrostatic forces dominate in

microassembly whereas gravity and physics are primary considerations in macro assembly.

The lack of effective tools and assembly strategies has resulted in lengthy time required for microsystem assembly.

Despite the many differences between microassembly and traditional assembly in methodologies and tools, major steps are quite similar between the two scales in automated assembly. These steps include:

1. Part feeding: Some of the part feeding techniques such as the common tape-bonded feeders used in microelectronics can be adopted in microsystem assembly.
2. Part grasping: Micro grippers, manipulators, and robots are desirable tools for this task. However, these tools cannot function properly for handling minute parts without intelligent end effectors. An intelligent end effector requires the integration of gripping, positioning, sensing, and orientation for accurate alignment in microscale of mating parts.
3. Part mating: At the micrometer scale, electrostatic and chemical forces dominate the interaction between grippers and parts, as well between the mating parts. Special design of grippers that can discharge these forces for possible stiction is necessary for easy release of parts from the gripper and for mating of small components.
4. Part bonding and fastening: Most of the bonding techniques involve microfabrication processes. Automated assembly is possible with batch fabrication of the bonding parts. Other methods of joining parts, including pulsed laser deposition, welding, soldering, "snap-fits" based on surface chemistry, and thin-film chemistry can be used for fastening microparts.
5. Sensing and verification: Three-dimensional machine vision systems such as stereo microscopy are effective for visual identification of parts and for part alignment. Other types of microsensors, e.g., tactile and thermal sensors, are also required in assembly and inspection. Near- and far-field infrared (IR) sensors can be used for microthermal feedback for monitoring welds or solder joints. Ideally these sensors should be integrated with the grippers and/or other process tooling.One common problem with most of these

sensors is the short depth of field near the wavelength of the light source in optical sensing systems. Another problem is the requirement for the sensing head to access the parts that need to be sensed.

As in traditional automated assembly, both serial and parallel assembly processes have been used in microassembly. Self-assembly is an attractive option for free-form fabrication of certain component groups of a microsystem.Parallel assembly is attractive for mass production of microsystems.

Overview of MEMS areas

RFMEMS

RF MEMS refers to the design and fabrication of dedicated MEMS for RF (integrated) circuits. There are various types of RF MEMS components, such as RF MEMStunableinductors, RF MEMSswitches,switched capacitorsandvaractors. RF MEMS components are fragile and require wafer level packaging or single chip packaging which allow for hermeticcavitysealing.They are biased electrostatically using a bipolarNRZdrive voltage, in order to avoiddielectric chargingand to increase the lifetime of the device.

Capacitive RF MEMS switches

RF MEMS switches are the specific micromechanical switches that are designed to operate at RF to mm wave frequencies. MEMS switches provide high isolation when open, low insertion loss when closed, and can be operated at low power consumption. Because of electromechanical isolation, the RF circuit doesn't leak or couple significantly to the actuation circuit.. Radio Frequency Micro Electro Mechanical Switches (RF MEMS) classification depends on the type of actuation, deflection axis, contact type, circuit configuration, and structure configuration. The most used RF MEMS mechanical structures are the cantilever beam and the air bridge structures.

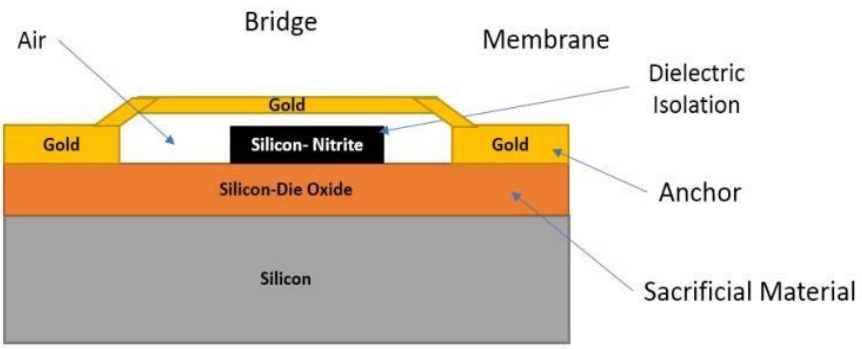
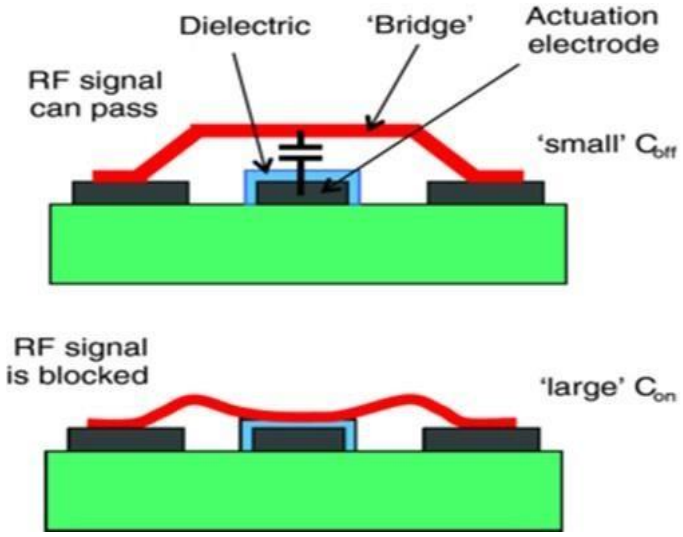


Fig: Capacitive RF MEMS switch

An air bridge base capacitive RF MEMS is shown here. Gold (Au) is used as a beam material, and Silicon Nitride (Si_3N_4) with dielectric constant 8.5 is used as a dielectric material. Silicon nitride thin film dielectrics are used in capacitive radio frequency microelectromechanical systems (MEMS) switches since they provide a low insertion loss, good isolation, and low return loss. A capacitor is built up between the fixed electrode and movable electrode



In air bridge type MEMS switch, beam is fixed at both the ends and voltage is applied in the middle of the beam to note down the displacement of the beam towards substrate. The displacement is maximum when we go on increasing the applied voltage. The actuation voltage

or applied voltage or pull in voltage is the maximum voltage at which the electrostatic force becomes superior over mechanical restoring force, causes pulling down of MEMS device towards the ground plane. Initially the applied input voltage is 1mv, there is no deformation in the switch under this condition (input is equal to output). But in the second case a 5v is added to 1mv,then some electrostatic force is created between the electrodes resulting in the deformation of cantilever and it touches the ground (output is zero).

RF MEMS Capacitor

The capacitors usually used in RF MEMS are variable type capacitor. The capacitance is given by $C = \frac{\varepsilon A}{d}$ .This capacitance can be tuned by changing either area , distance between the plates, or the dielectric constant.Therefore RF MEMS tunable capacitors are categorized according to their tuning parameters:

- MEMS gap-tuning capacitors;
- MEMS area-tuning capacitors;
- MEMS dielectric tunable capacitors.

The gap-tuning capacitors can be made with two parallel electrodes. The lower electrode is fixed while the upper is connected to a spring and is movable. The gap between the electrodes changes with change in applied voltage. This principle can be implemented with three plates, the middle one being movable and the other two being fixed. The bridge switch can be used also as a variable capacitor.

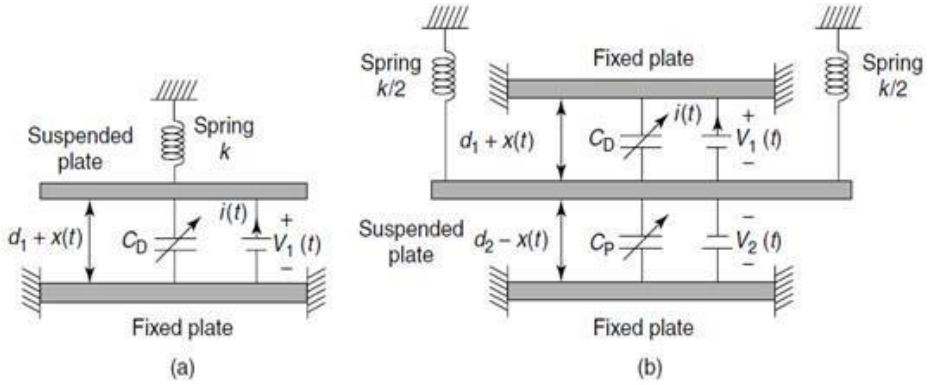


Fig: Gap tuning capacitors

Comb like interdigitabletunable capacitors

The most common area tuning capacitor is the interdigital comb structure capacitor.One finger is fixed while the other is moving. The tuning range is determined by the finger length.

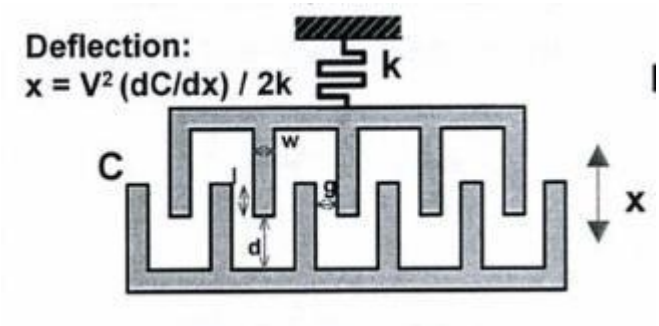


Fig: Comb like interdigitabletunable capacitors

The interdigital structure can also be used as dielectric tunable capacitor. Both combs can be fixed. The dielectric material (STO), grows in size as the temperature increases. Hence its dielectric constant changes.

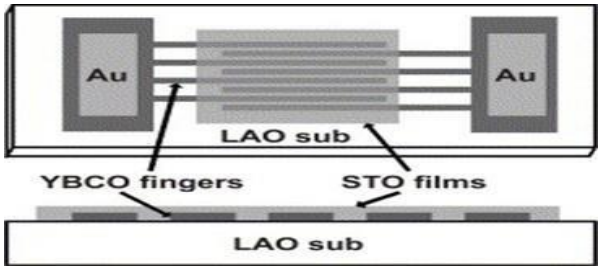


Fig : Dielectric Tunable capacitors

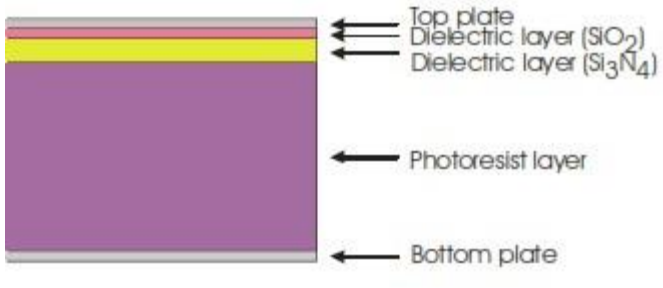


Fig: Cross section of RF MEMS capacitor

RF MEMS capacitor networks presented here are based on two-plate capacitors with dielectric materials in between. Membranes included in the design are held by four suspensions. The total capacitance is obtained from two different sections. The first section is with solid dielectric media and photoresist layer, and the second one is with the dielectric media and additional air gap. The dielectric medium consists of SiO_2, Si_3N_4 and an air gap. The combination of SiO_2 and Si_3N_4 is used to compensate unwanted mechanical strain effect. In order to have an air gap, a photoresist layer, used as a sacrificial layer, is deposited and is later removed at the end of the process.

BioMEMS

The term "BioMEMS" has been a popular terminology in the MEMS industry in recent years.

BioMEMS include the following three major areas:

- Biosensors for identification and measurement of biological substances,
- Bioinstruments and surgical tools, and
- Bioanalytical systems for testing and diagnoses.

These sensors are extensively used in medical diagnosis, environmental protection, drug discovery and delivery, etc.

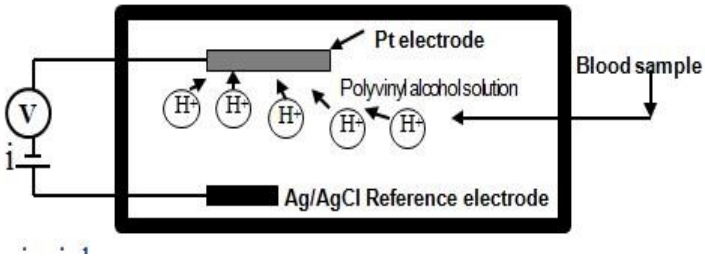
Biomedical Sensors are used to measure biological substances as well as for medical diagnosis purposes.Biomedical Sensors These sensors can analyze biological samples in quick and accurate ways. These miniaturized biomedical sensors have many advantages over the traditional instruments. They require typically a minute amount of samples and can per form analyses much faster with virtually no dead volume

Working principle:

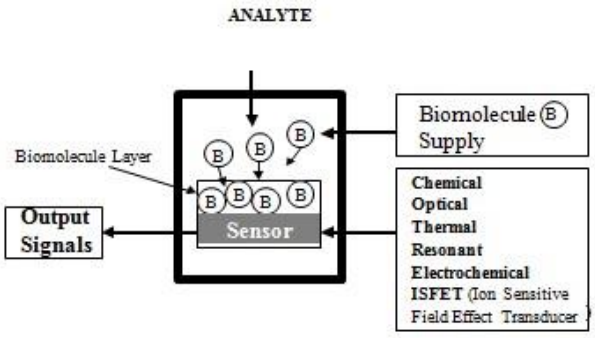
A small sample of blood is introduced to a sensor with a polyvinyl alcohol solution. Two electrodes are present in the sensor: a platinum film electrode and a thin Ag/AgCl film (the reference electrode. The glucose in patient's blood sample reacts with the O_2 in the polyvinyl alcohol solution and produces H_2O_2. Glucose $+O_2 \rightarrow$ gluconolactone + H_2O_2

The H_2 in H_2O_2 migrates toward Pt film in a electrolysis process, and builds up layers at that electrode.

The difference of potential between the two electrodes due to the build-up of H_2 in the Pt electrode relates to the amount of glucose in the blood sample.



Biosensorswork on the principle of the interaction of the analytes that need to be detected with biologically derived biomolecules, such as enzymes of certain forms, antibodies, and other forms of protein. These biomolecules, when attached to the sensing elements, can alter the output signals of the sensors when they interact with the analyte



Proper selection of biomolecules for sensing elements (chemical, optical etc) can be used for the detection of specific analyte

MOEMS

Micro Opto Electro Mechanical systems (MOEMS) are a special class of Micro-electromechanical systems (MEMS) which involves sensing or manipulating optical signals on a very small size scale using integrated mechanical and electrical systems. MOEMS includes a wide variety of devices including optical switch, optical cross-connect, tunable VCSEL, microbolometers amongst others. These devices are usually fabricated using standard micromachining technologies using materials like silicon, silicon dioxide, silicon nitride and gallium arsenide. The digital micromirror device, or DMD, is themicro-opto-electromechanical system(MOEMS) that is the core of the trademarked DLP projection technology fromTexas Instruments.

Micro-optical switches

The direction in which the light beam is reflected can be changed by rotating the mirror to different angles, allowing the input light to be connected to any output port. In a MEMS optical switch, a micro-mirror is used to reflect a light beam. This type of optical switch has been realized for the first time through the fusion of various techniques such as micro-machining techniques for fabricating the mirror, optical design techniques for achieving low-loss optical connections, and control techniques for positioning the mirror accurately. Since this device can switch large numbers of optical signals simultaneously, it can be used as a trunk switch for handling large amounts of traffic, and as a switch in large urban communication networks.

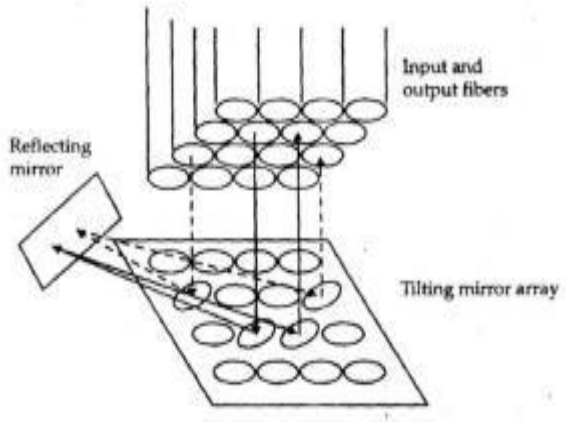
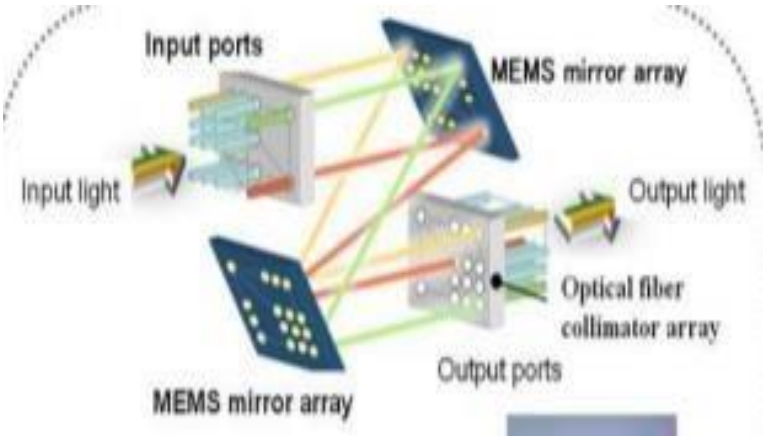


Fig: Principle of MOEMS



MEMS Tunable VCSEL

Vertical Cavity Surface Emitting Lasers (VCSELs) are semiconductor-based devices that emit light perpendicular to the chip surface. VCSELs were originally developed as low-cost, low-power alternatives to edge-emitting diodes, mainly for high-volume datacomapplications.MEMS-tunable VCSELs utilize microelectromechanical mirror systems (MEMS) to vary the cavity length of the laser, thereby tuning the output wavelength. The limited tuning range and output power of these devices have precluded them from being used in OCT (Optical coherence tomography) applications.

In order for a MEMS-tunable VCSEL to be successful for applications in OCT, it needs to meet certain standards:

- Rapid Sweep Speed
- Broad Tuning Range
- Long Coherence Length
- High Laser Output Power

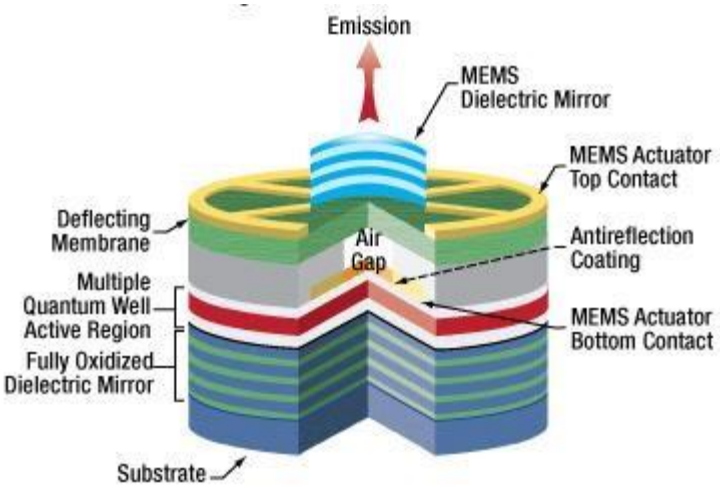


Fig: 3D view of MEMS Tunable VCSEL

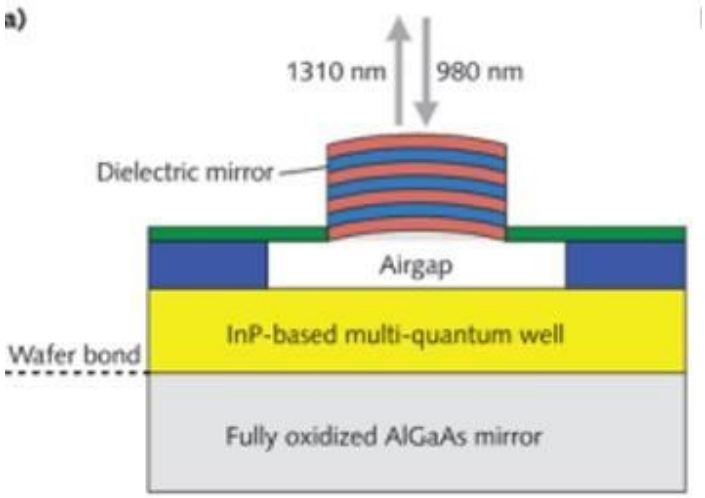


Fig : MEMS Tunable VCSEL

The tunable VCSEL is constructed by bonding a wide-gain, indium phosphide (InP)-based quantum-well active region to a gallium arsenide (GaAs)-based oxidized mirror. An electrostatically actuated dielectric mirror suspended over the top of this structure and separated by an air gap moves to generate 1310 nm tunable emission as the device is pumped by a 980 nm laser source. The emission is then coupled to a broadband semiconductor optical amplifier, which not only increases output power but also shapes the spectral output of the tunable VCSEL before it is input to an OCT system.

NEMS

Nanoelectromechanical systems (NEMS) are a class of devices integrating electrical and mechanical functionality on thenanoscale. NEMS form the next logical miniaturization step from so-called MEMS.NEMS typically integrate transistor-likenanoelectronicswith mechanical actuators, pumps, or motors, and may thereby form physical, biological, andchemical sensors. The name derives from typical device dimensions in thenanometerrange, leading to low mass, high mechanical resonance frequencies, largequantum mechanicaleffects and a high surface-tovolume ratio useful for surface-based sensing mechanisms.A key application of NEMS isatomic force microscopetips. The increased sensitivity achieved by NEMS leads to smaller and more efficient sensors to detect stresses, vibrations, forces at the atomic level, and chemical signals.Many of the commonly used materials for NEMS technology have beencarbonbased, specificallydiamond,carbon nanotubesandgraphene. This is mainly because of the useful properties of carbon based materials which directly meet the needs of NEMS.

Nanoelectromechanical relay

A nanoelectromechanical (NEM) relay is an electrically actuatedswitchthat is built on thenanometerscale usingsemiconductor fabricationtechniques. They are designed to operate in replacement, or in conjunction, with traditionalsemiconductorlogic. While the mechanical nature of NEM relays makes them switch much slower thansolid-state relays, they have many advantageous properties, such as zerocurrent leakageand lowpower consumption. A typical NEM Relay requires a potential on the order of the tens of volts in order to "pull in" and havecontact resistanceson the order of gigaohms.

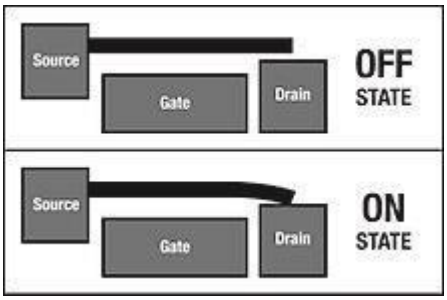


Fig: Schematic of a three terminal electromechanical relay

A NEM relay can be fabricated in two, three, or four terminal configurations. A three terminal relay is composed of a source (input), drain (output), and a gate (actuation terminal). Attached to the source is acantileveredbeam that can be bent into contact with the drain in order to make an electrical connection. When a significantvoltagedifferential is applied between the beam and gate, and theelectrostaticforce overcomes theelastic forceof the beam enough to bend it into contact with the drain, the device "pulls in" and forms an electrical connection. In the off position, the source and drain are separated by an air gap. This physical separation allows NEM relays to have zerocurrentleakage, and very sharp on/off transitions.

The nonlinear nature of the electric field, andadhesionbetween the beam and drain cause the device to "pull out" and lose connection at a lower voltage than the voltage at which it pulls in. Thishysteresiseffect means there is a voltage between the pull in voltage, and the pull out voltage that will not change the state of the relay, no matter what its initial state is. This property is very useful in applications where information needs to be stored in the circuit, such as instatic random-access memory.

Nanoelectromechanichal switched capacitor

Consider a nanoelectromechanical (NEM) device consisting of a source, a drain and a gate electrode. A vertically aligned multiwalled carbon nanotube (MWCNT) was grown on the source electrode and was coated with a dielectric layer (SiN_x) and a metal layer (Cr) to form a CNT– insulator– metal (CIM) capacitor. The MWCNT grown on the drain electrode is the mechanically active element of the cell; electrostatic forces cause it to bend and make contact with the CIM structure on the source.There is no nanotube on the gate electrode.

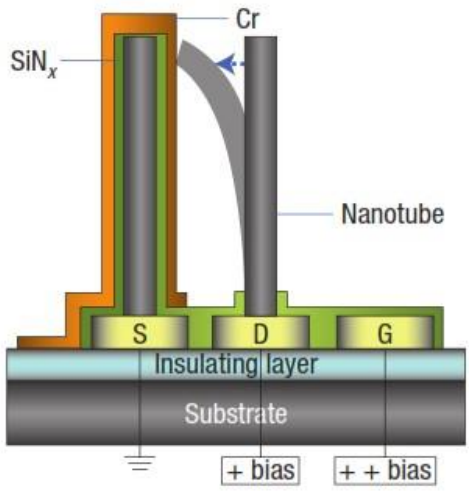


Fig: Switched capacitor

In operation, the source is electrically connected to ground, the drain is connected to the bit line, which has a constant positive voltage applied to it, and the gate is connected to the word line. When this word line is positively biased (to a value higher than the bit line voltage), the nanotube on the drain experiences a repulsive electrostatic force from the gate electrode and an attractive electrostatic force from the source electrode, causing it to deflect until it makes contact with the metal electrode on the capacitor .On contact, a transient current flows to charge the CIM capacitor. This charge is used to represent a bit of stored information. When the gate bias is removed, the electrostatic force giving rise to the deflection of the drain MWCNT is also removed, and the nanotube springs back to the non-contact 'OFF' position.

PREVIOUS YEAR KTU QUESTIONS

1. What is meant by BioMEMS. Discuss the challenges involved in BioMEMS. List three applications of BioMEMS
2. Explain anodic bonding and Silicon Fusion Bonding
3. Explain with figures two applications which use NEMS technology

4. Explain with figures two RF MEMS applications
5. Explain the bonding techniques with figures a) Silicon-on-Insulator b) Wire bonding
6. Explain any one application of MOEMS with figures
7. Explain anodic bonding

PREVIOUS UNIVERSITY QUESTIONS

1. List a few RF MEMScomponents and give their applications
2. Write notes on optical MEMS
3. Explain the working of any two RF MEMS components and give their applications

V	Overview of Micro manufacturing – Bulk micro manufacturing, Surface micro machining , LIGA process –Microstereo lithography	6	20%
	Micro system Packaging: general considerations in packaging design – Levels of Micro system packaging	3	

Overview of Micro manufacturing

Micromachining is considered as a process as well as a technology that is utilized to structure wafer materials or thin films in order to fabricate miniature devices such as microsensors, microactuators and passive components for microsystem functioning. Three distinct micromachining techniques are

1. Bulk micro manufacturing
2. Surface micromachining
3. LIGA process

Bulk micro manufacturing

Bulk micro manufacturing involves the removal of materials from the bulk substrates either by dry or wet etching, to form the desired three dimensional geometry of the microstructures. This method is widely used in the production of microsensors and accelerometers. Etching, either the orientation independent isotropic etching or the orientation dependent anisotropic etching, is the key technology used in bulk micro manufacturing. Substrates commonly used are SiC, GaAs and quartz.

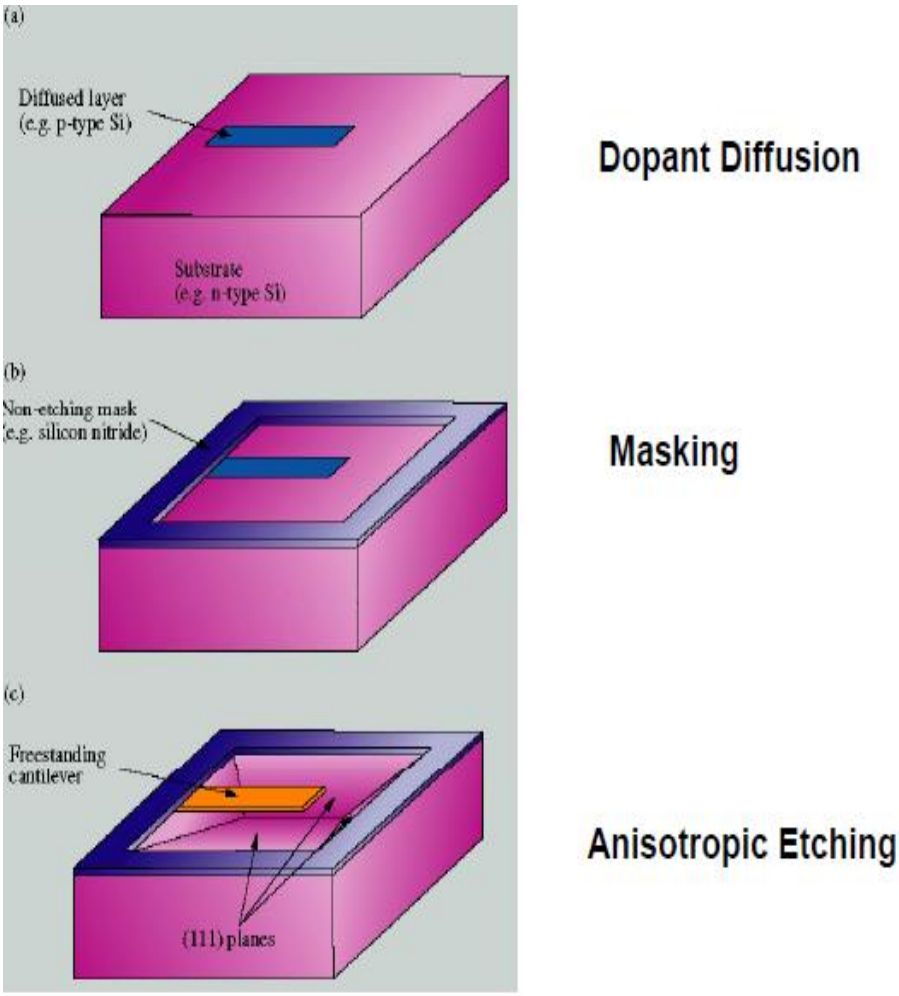


Fig: Cantilever beam produced by Bulk micromachining

Isotropic and Anisotropic etching

For substrates made of homogeneous and isotropic materials, the chemical etchantswill attack the material uniformly in all directions. Thisorientation-independent etching is referred to as isotropic etching.

Isotropic etching is hardly desirable in micromanufacturing because lack of control of the finished geometry of the workpiece Most substrate materials are not isotropic in their crystalline structures. Therefore, some parts in the crystalare stronger, and thus more resistant to etching, than others. Three planes of silicon crystals such as (100), (110), and (111) are of particular importance in micromachining. The three orientations <100>, <110>, and <111> are the respective normal lines to the (100), (110), and (111) planes. In micromachining, the <110>

orientation is the favored orientation. This is because, in this orientation, the wafer breaks or cleaves more cleanly than in the other orientations. The (110) plane is the only plane in which one can cleave the crystal in vertical edges. The (111) plane is the toughest plane to treat. Thus <111> orientation is the elast used orientation in micromachining.

Despite the many advantages of anisotropic etching in controlling the shape ofthe etched substrates, there are several disadvantages: (1) It is slower than isotropicetching: the rate rarely exceeds 1 μm/min. (2) The etching rate is temperature sensitive. (3) It usually requires an elevated temperature around 100°C in the process.

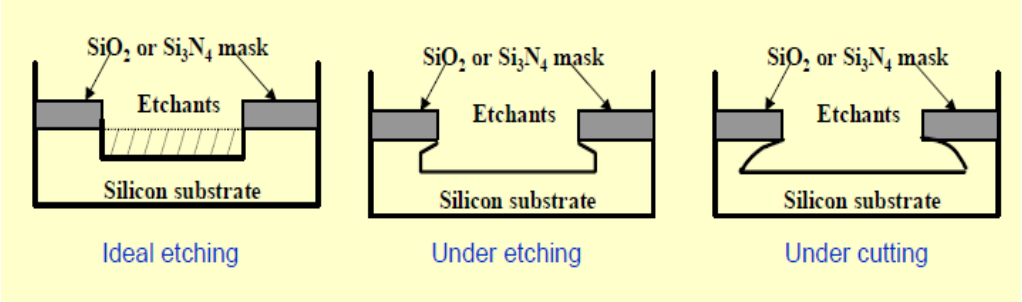
Wet etchants

The common isotropic etchant for silicon is called HNA, whichdesignates acidic agents such as $HF/HNO_3/CH_3COOH$. These etchants can be usedeffectively at room temperature. Alkaline chemicals with pH> 12 are used for anisotropic etching. Popular anisotropic etchants for silicon include potassium hydroxide (KOH), ethylene-diamine and pyrocatechol (EDP), tetramethyl ammonium hydroxide (TMAH), and hydrazine. Most etchants based on theabove chemicals are diluted with water, normally 1:1 by weight.

Silicon compounds are much stronger etching resistive materials than silicon.These materials can thus be used as masks for etching of silicon substrates. The resistivity to etchants is measured by selectivity ratioof a material which is defined as

$$\text{Selectivity ratio}=\frac{\text{Etching rate of silicon}}{\text{Etching rate of the material}} \quad \text{using same etchants}$$

The higher the selectivity ratio, the better the mask material is. However, the timing of etching and the agitated flow patterns of the etchants over the substrate surfaces need to be carefully controlled in order to avoid serious under etching and undercutting



Etch stop

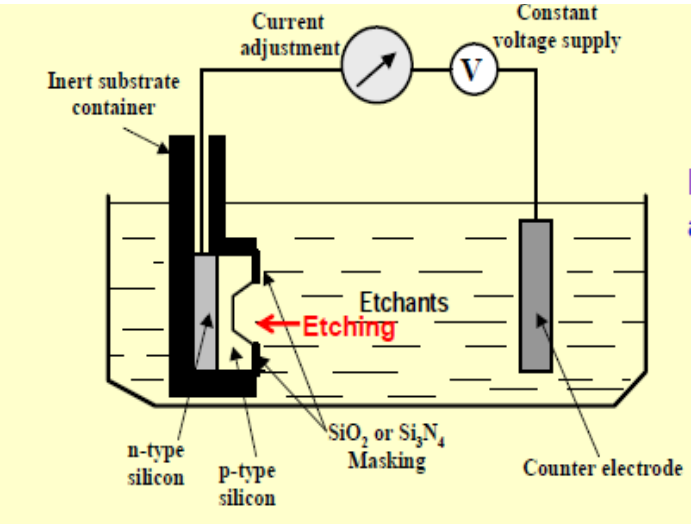
There are two popular techniques used in etch stop. These are (1) dopant-controlledetch stop and (2) electrochemical etch stop

Dopant controlled etch stop

A peculiar phenomenon that can be used tocontrol the etching of silicon is that doped silicon substrates, whether they are dopedwith boron for p-type silicon or phosphorus or arsenic for n-type silicon, show a different etching rate than pure silicon. In the case when then isotropic HNA etchant areused, the p- or n-doped areas are dissolved significantly faster than the undoped regions.

Electrochemical etch stop

This technique is popular for controlling anisotropic etching.A lightly doped p-n junction is first produced in the silicon wafer by a diffusion process. The doped silicon substrate is then mounted on an inert substrate container made of a material such as sapphire. The n-type silicon layer is used as oneof the electrodes in an electrolyte system with a constant voltage source. The unmasked part of the p type substrate face is in contact with the etchant. Etching thus takes place as usual until it reaches the interface of the p-n junction, at which point etching stops because of the rate difference in p- and n-doped silicon. Consequently, one can effectively control the depth of etching simply by establishing the p-n silicon boundaries at the desired locations in a doped silicon substrate.



Dry etching

Dry etching involves the removal of substrate materials by gaseous etchant withoutwet chemicals or rinsing. Conventional dry etching is a very slow process, at a rate of about 0.1 μm/min or100 A/min.Dry etching of silicon substrates, such as by plasma, typically is faster and cleaner than wet etching. A typical dry etching rate is 5μm/min, which is about 5 times that of wet etching. Like wet etching, dry etching also suffers the shortcoming of being limited to producing shallow trenches. Consequently, both wet anddry etching processes are limited to producing MEMS with low aspect ratios. The aspect ratio (A/P) of a MEMS component is defined as the ratio of its dimension inthe depth to those in the surface. For dry etching, the A/P is less than 15. Anotherproblem with dry etching relates to the contamination of the substrate surface byresidues.

There are three dry etching techniques: **plasma, ion milling and reactive ion etch (DRIE)**

Plasma etching

Plasma is a neutral ionizedgas carrying a large number of free electrons and positively charged ions. A commonsource of energy for generating plasma is a radio-frequency (RF) source. The processinvolves adding a chemically reactive gas such as CCl_2F_2, to the plasma, one that contains ions and has its own carrier gas (inert gas such as argon gas).The reactive gasproduces reactive neutrals when it is ionized in theplasma. The reactive neutrals bombard the target on both the sidewalls as well as thenormal surface, whereas the charged ions bombard only the normal surface of thesubstrate. Etching of the substrate materials is accomplished by the high-energy ionsin the plasma bombarding the substrate surface with simultaneous chemical reactionsbetween the reactive neutral ions and the substrate material. This high-energy reaction causes local evaporation, and thus results in the removal of the substrate material. The etching front moves more rapidly in the depthdirection than in the direction of the sidewalls. This is due to the larger number of high-energy particles involving both the neutral ions and the charged ions bombarding the normal surface, while the sidewalls are bombarded by neutral ions only. Plasma etching is normally performed in high vacuum.

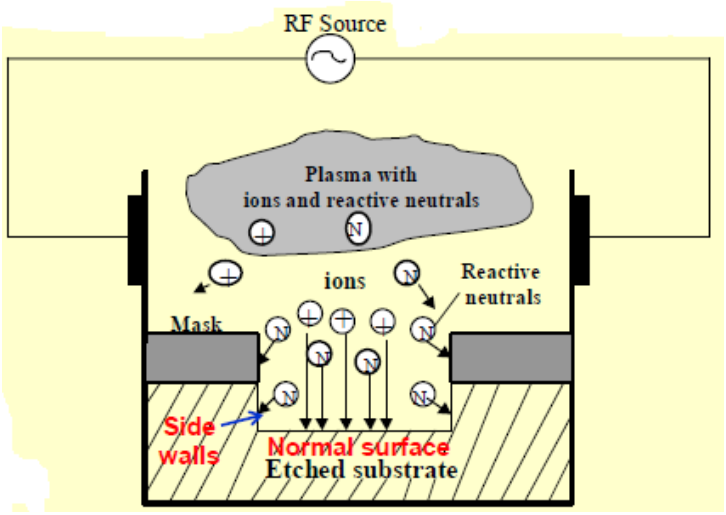


Fig : Plasma etching

Plasma etching can increase the etching rates in the order of 2000 A/min.This increase in etching rate is primarily due to the increased mean free path of thereacting gas molecules in the depth to be etched.

Deep reactive Ion Etching (DRIE)

Despite the significant increase in theetching rate and the depth of the etched trench or cavity that can be achieved with theuse of plasma, the etched walls in the trenches remain at a wide angle (θ) to its depth.

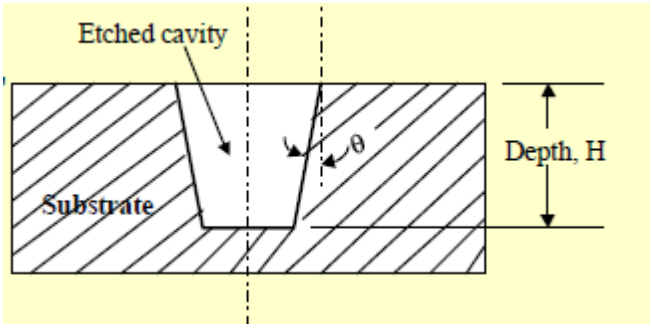


Fig : sidewall angle in an etched cavity

The cavity angle θ is critical in many MEMS structuressuch as the comb electrodes in the microgripperswherethe faces of the electrodes, or "fingers" must be parallelto each other.Etching processes produce most of these comb electrodes. It ishighly desirable that the angle θ be kept at a minimum in deep-etched trenches thatseparate the plate electrodes. Obtaining deep trenches

with vertical walls is a major drawback in bulk manufacturing. Consequently, the bulk manufacturing technique has been generally regarded as suitable only for MEMS with low aspect ratios, with tapered cavity walls.

Deep reactive ion etching (DRIE) is a process that can overcome the problemdescribed above. The DRIE process has since extended the use of the bulk manufacturing technique to the production of MEMS of high aspect ratio (A/P) with virtuallyvertical walls; ie., $\theta \approx 0$.

The DRIE process differs from dry plasma etching in that it produces thin protective films of a few micrometers on the sidewalls during the etching processes.It involves the use of a high-density plasma source, which allows alternating processes of plasma (ion) etching of the substrate material and the deposition of etching-protective material on the sidewalls as illustrated in Figure.Suitable etching protective materials (shown in black in the figure) are those materials of high selectivity ratio, such as silicon dioxide.Polymers are also frequently used for this purpose. The DRIE process with polymeric sidewall protection has been used to produce MEMS structures with A/P = 30 with virtually vertical walls of$\theta = \pm 2^0$.

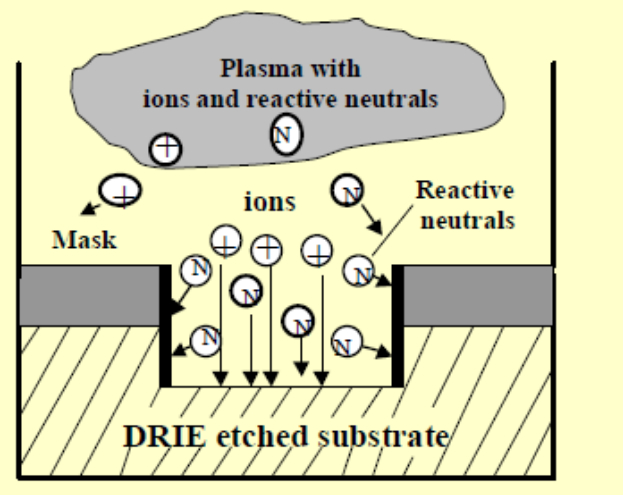


Fig : DRIE process

There are a number of reactant gases that could be used in DRIE. One of thesereactants is fluoropolymers (nCF_2) in the plasma of Argon gas ions. This reactant canproduce a polymer protective layer on the sidewalls while etching takes place. Therate of etching is in the range of 2 to 3 µm/min, which is higher than what wet etching can accomplish.

Comparison of Wet versus Dry etching

Parameters	Dry etching	Wet etching
Directionality	Good for most materials	Only with single crystal materials (aspect ratio up to 100)
Production-automation	Good	Poor
Environmental impact	Low	High
Masking film adherence	Not as critical	Very critical
Selectivity	Poor	Very good
Materials to be etched	Only certain materials	All
Process scale up	Difficult	Easy
Cleanliness	Conditionally clean	Good to very good
Critical dimensional control	Very good (< 0.1 μm)	Poor
Equipment cost	Expensive	Less expensive
Typical etch rate	Slow (0.1 μm/min) to fast (6 μm/min)	Fast (1 μm/min and up)
Operational parameters	Many	Few
Control of etch rate	Good in case of slow etch	Difficult

Advantages

- Straightforward, involving well-documented fabrication processes.
- Less expensive in the process, but material loss is high.
- Suitable for simple geometry

Disadvantages

- Limited to low-aspect ratio in geometry; wafers.
- Wastage of material is more

SURFACE MICROMACHINING

The surface micromachining technique builds microstructure by adding materials layer by layer on top of the substrate. Low pressure chemical vapor deposition (LPCVD) techniques are used for such builders, and polycrystalline silicon (polysilicon) is a common material for the

layer material.Sacrificial layers, usually made of SiO_2, are used in constructing the MEMS components but are later removed to create necessary void space in the depth. Wet etching is the common method used for this purpose. Layers that are being added in surfacemicromachining are typically 2 to 5 μm thick each. During manufacturing surface micromachining not only saves material, but also eliminates the need for a die attach.

Process

Surface-micromachined devices are typically made up of three types of components

(1) a sacrificial component (also called a spacer layer),

(2) a microstructural component, and

(3) an insulator component.

The sacrificial components are usually made of phosphosilicate glass (PSG) or SiO_2 deposited on substrates by LPCVD techniques. PSG can be etched more rapidly than SiO_2 in HF etchant. These components in the form of films can be as long as 1 to 2000 μm and 0.1 to 5 μm thick. Both microstructural and insulator components can be deposited in thin films. Polysilicon is a popular material. The etching rates for the sacrificial components must be much higher than those for the two other components.

The construction of microcantilever beam by the surface micromachining technique is shown in figure.

Step 1 PSG is deposited on the surface of silicon substrate base

Step 2 A mask (mask 1) is made to cover the surface of the PSG layer

Step 3 Etching is carried out for attaching the future cantilever beam

Step 4 Another mask (mask 2) is made for the deposition of polysilicon microstructural material

Step 5 Using mask polysilicon is deposited over the PSG layer

Step 6 The PSG that remains in step 5 is subsequently etched away to produce the desired cantilever beam. After etching, the structure is rinsed in deionized water thoroughly followed by drying under infrared lamps. The most suitable etchant for the sacrificial PSG layer is 1:1 HF, which is made of 1:1 HF:H_2O+ 1:1 HCl:H_2O.

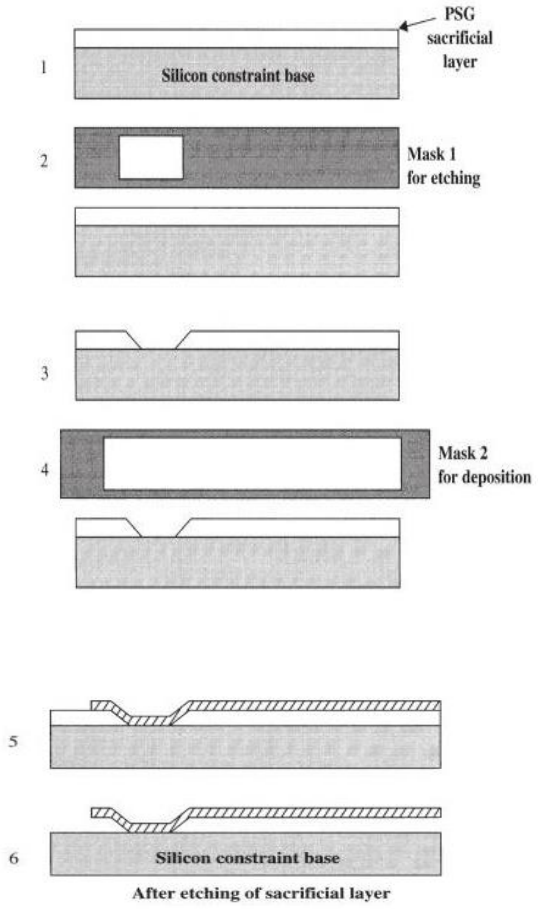
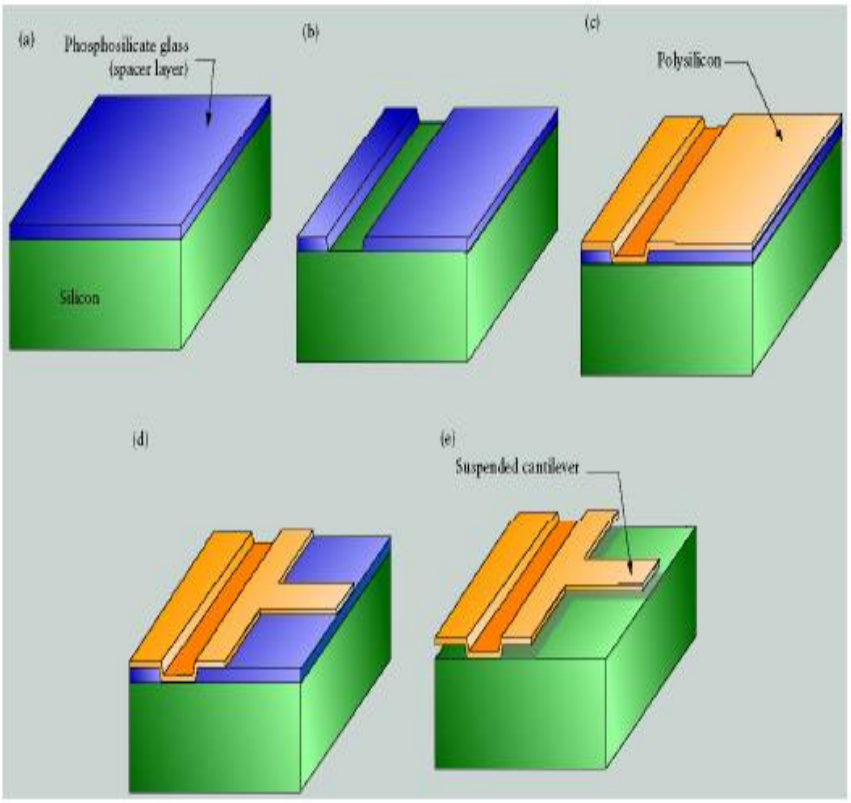


Fig : Surface micromachining process



(a) deposition of a phosphosilicate glass (PSG) spacer later; (b) etching of the spacer layer; (C) deposition of polysilicon; (d) etching of polysilicon; (e) selective wet etching of PSG, leaving the silicon substrate and deposited polysilicon unaffected

Advantages

- not constrained by the thickness of silicon wafers:
- wide choices of thin film materials to be used;
- suitable for complex geometries such as microvalves and actuators

Disadvantages

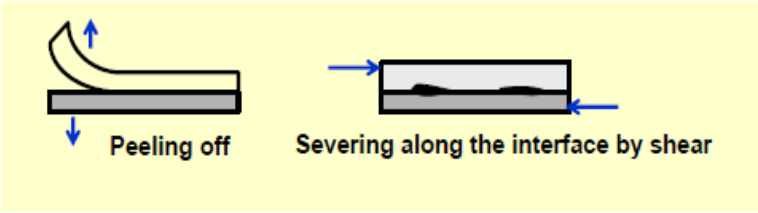
- Requires the building of layers of materials on the substrate
- Complex masking design and productions
- Etching of sacrificial layer is necessary.
- The process is tedious and more expensive.
- There are serious engineering problems such as interfacial stresses and stiction

Mechanical Problems Associated with Surface Micromachining

Three major mechanical problems of surface micromachining are (1) adhesion of layers, (2) interfacial stresses, and (3) stiction.

Adhesion of Layers

Whenever two layers of materials, whether similar or dissmilar, are bonded together, a possibility of delamination exists. A bilayer structure can delaminate at the interface either by peeling of one layer from the other or by shear that causes the severing of the interfaces locally along the interface. Excessive thermal and mechanical stress is the main cause for interfacial failures. However, other causes including the surface conditions, e.g.the cleanliness, roughness, and adsorption energy, could also contribute to the weakening of the interfacial bonding strength.

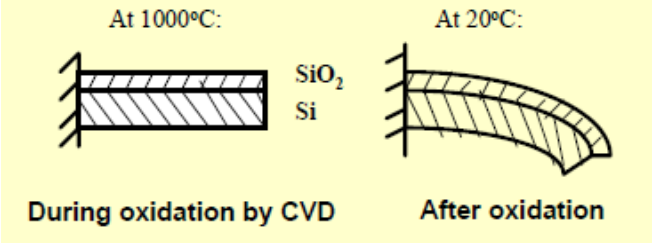


Interfacial stresses

There are typically three types of stresses that exist in the bilayer structures. The most obvious one is the **thermal stresses** resulting from the mismatch of the coefficients of thermal expansion (CTE) of the component materialals. Severe thermal stress can cause the delamination of the SiO_2 layer from the silicon substrate when the bilayer structure is subjected to high enough operating temperature.

The second type of interfacial stresses is the **residual stresses** that are inherent in the microfabrication processes. A SiO_2, layer grown on the top surface of a silicon substrate beam at 1000°C by a thermal oxidation process is shown in Figure (a). The resultant shape of the bilayer beam at room temperature will be that shown in Figure (b) because of the significant difference

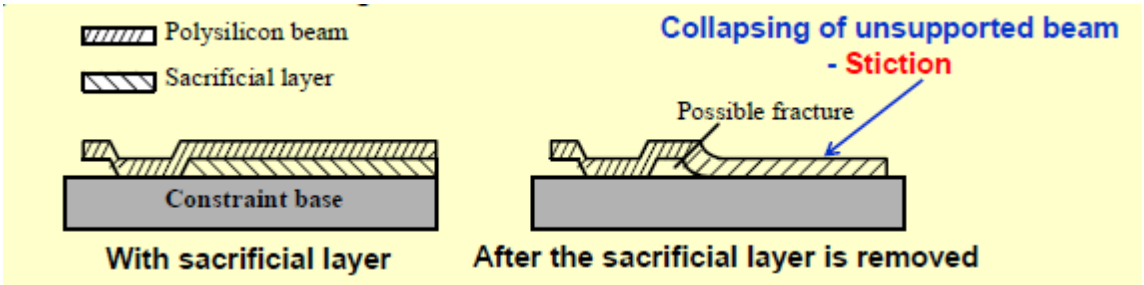
in the CTE for both materials. Excessive tensile residual stress in SiO_2 layer can cause multiple cracks in the layer.



The third type of stress that could be introduced in thin-film structures is the **intrinsic stress** due to local change of atomic structure during microfabrication processes.

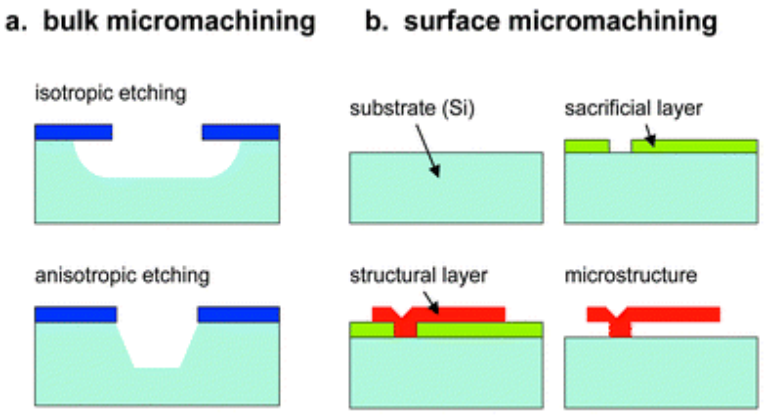
Stiction

The phenomenon of two separated pieces sticking together is called stiction. It often occurs when the sacrificial layer is removed from the layers of material. The thin structure that was once supported by the sacrificial layer may collapse on the other material. As in figure stiction could happen with the thin polysilicon beam dropping onto the top surface of the silicon substrate (the constraint base) after the removal of the sacrificial PSG layer. The two materials would then stick together after the joint. Considerable mechanical forces are required to separate the two stuck layers again and these excessive forces can break the delicate microstructure. Stiction is the main cause for the large amount of scraps in surface micromachining. Stiction occurs due to Van der Waals and chemical forces between surfaces with narrow gaps.



Comparison of bulk and surface micromachining

	Bulk Micromachining	Surface Micromachining
1	Large features with substantial mass and thickness	Small features with low thickness and mass
2	Utilizes both sides of the wafer	Multiple deposition and etching required to build up structures
3	Vertical dimensions one or more wafer thickness	Vertical dimensions are limited to the thickness of the deposited layer leading to compliant suspended structures with the tendency to stick to the support
4	Generally involves laminating Si wafer to Si or glass	Surface micromachined device has its built-in support and is more cost effective
5	Piezoresistive or capacitive sensing	Capacitive and resonant sensing mechanisms
6	Wafers may be fragile near the end of the production	Cleanliness critical near end of process
7	Sawing, packaging, testing is difficult	Sawing, packaging, testing is difficult
8	Some mature products or producers	No mature products or producers
9	Not very compatible with IC technology	Natural but complicated integration with circuitry: integration is often required due to the tiny capacitive signals



LIGA process

The term LIGA is an acronym for the German terms Lithography (Lithographphie), electroforming (Galvanoformung), and molding (Abformung). The technique was first developed at the Karlsruhe Nuclear Research Center in Karlsruhe, Germany. Non silicon based microstructures can be manufactured by this process. Nickel is a common material for LIGA products. Using LIGA, microstructures with high aspect ratio can be produced.

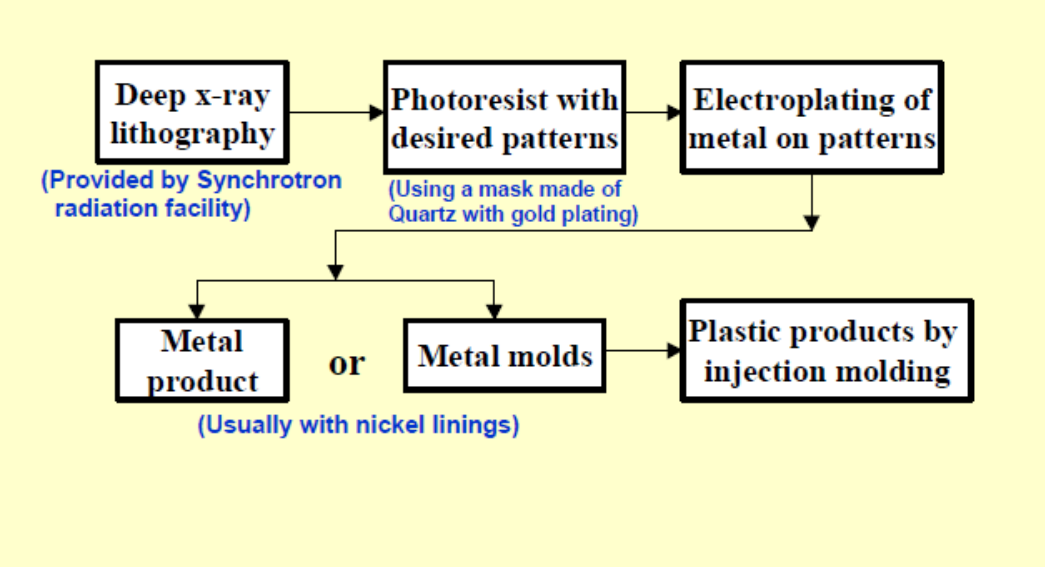


Fig: Major fabrication steps

The LIGA process begins with deep x-ray lithography that sets the desired patterns on a thick film of photoresist. The X-rays used in this process are provided by a synchrotron radiation source, which allows a high throughput because the high flux of collimated rays shortens the exposure time. X-rays are used as the light source in photolithography because of their short wavelength, which provides higher penetration power into the photoresist materials. This high penetration power is necessary for high resolution in lithography, and for a high aspect ratio in the depth.

Substrate materials for LIGA

The substrate used in LIGA is often called as base plate. It must be an electrical conductor, or an insulator coated with electrically conductive materials. Electrical conduction of the substrate is necessary in order to facilitate electroplating, which is a part of the LIGA process. Suitable materials for the substrates include: austenite steel; silicon wafers with a thin titanium or Ag/Cr top layer; and copper plated with gold, titanium, and nickel. Glass plates with thin metal plating could also be used as the substrate.

Photoresist Materials

Basic requirements for photoresist materials for the LIGA process include the following:

-It must be sensitive to X-ray radiation.

- It must have high resolution as well as high resistance to dry and wet etching.

-It must have thermal stability up to 140°C.

-The unexposed resist must be absolutely insoluble during development.

-It must exhibit very good adhesion to the substrate during electroplating.

Based on the requirements listed above, PMMA is considered to be an optimal choice of photoresist material for the LIGA process. However, its low lithographic sensitivity makes the lithographic process extremely slow. Another shortcoming of PMMA is its vulnerability to crack due to stress.

Fabrication

The desired product in this example is a microthin wall metal tube of square cross section. Deposit a thick film of photoresist material on the surface of a substrate as shown in Figure (a). A popular photoresist material that is sensitive to X-ray is poly methyl meth acrylate (PMMA). Masks are used in the x-ray lithography. Most masking materials are transparent to X-rays, so it is necessary to apply a thin film of gold to the area that will block x-ray transmission.

The thin mask used for this purpose is silicon nitride with a thickness varying from 1 to 1.5 µm. The deep X-ray lithography will cause the exposed area to be dissolved in the subsequent development of the resist material (Figure b). The PMMA photoresist after the development will have the outline of the product, i.e. the outside profile of the tube. This is followed by electroplating of the PMMA photoresist with a desired metal, usually nickel, to produce the tubular product of the required wall thickness (Figure c). The desired tubular product is produced after the removal of the photoresist materials (ie, PMMA) by oxygen plasma or chemical solvents. For most applications the desired product is metal molds for subsequent injection molding of microplastic products.

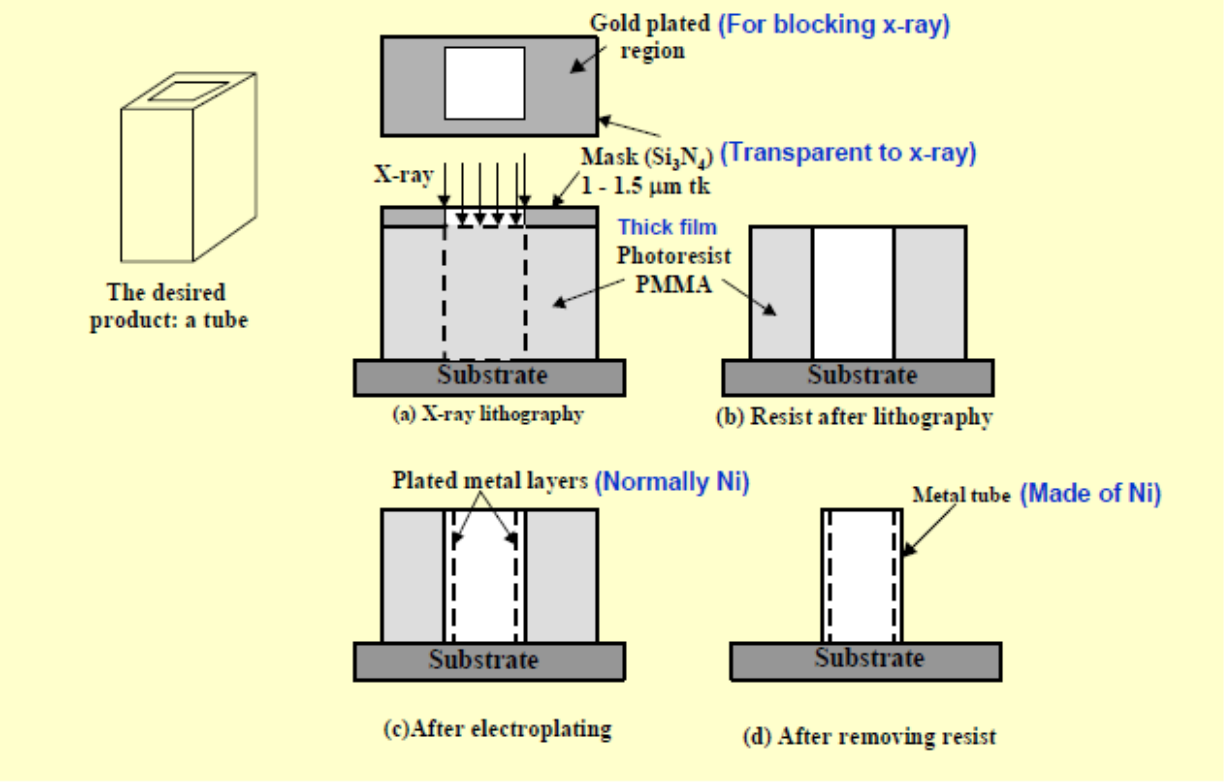


Figure: Major steps in LIGA process (eg:tube)

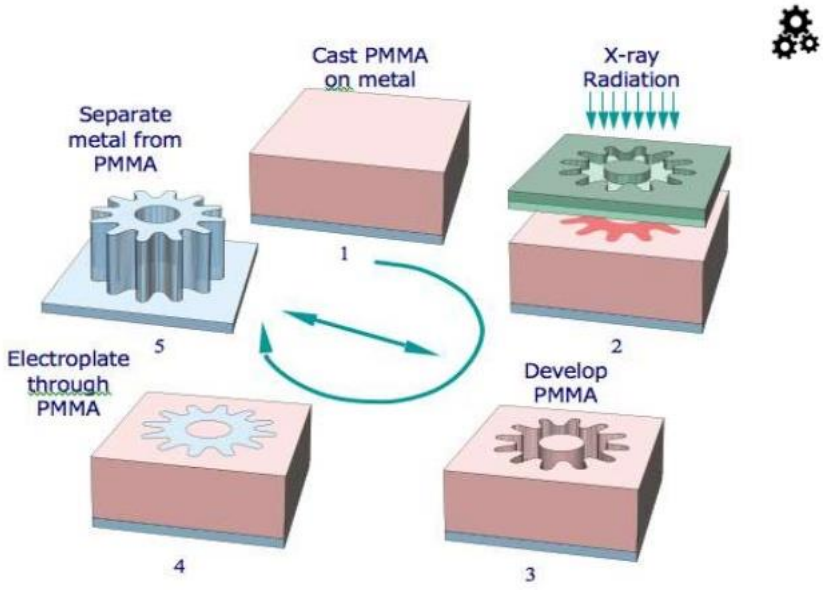


Figure: Major steps in LIGA process (eg: gear)

Advantages

- virtually unlimited aspect ratio of the microstructure geometry
- flexible microstructure configurations and geometry
- the only one of the three techniques that allows the production of metallic microstructures
- the best of the three manufacturing processes for mass production, with the provision for injection molding.

Disadvantages

- The most expensive process of all
- Requires a special synchrotron radiation facility for deep X-ray lithography
- Requires the development of microinjection molding technology and a facility for mass production purposes.

Microstereo lithography

Microstereo lithography is a novel microfabrication process for fabricating high aspect ratio and complex 3D microstructures on the μm - mm scale including curvilinear and re-entrant microstructures that are difficult to make using conventional micromachining.It is an enabling technology for making MEMS devices in materials other than silicon. It is sometimes referred to as “Poor mans LIGA process”.

The principle behind this process is whenever a photopolymer is exposed to light, it turns into solid. So selective exposure of liquid layer (photopolymer) to light is done.Using this complex 3-D structure is built layer by layer with one layer built on another. Motivation behind using this are the limitations of traditional processes such as:

- Inability to manufacture high aspect ratio and complex 3D microstructures. Conventional fabrication processes has capability to manufacture 2-D parts or planar components.
- Limitation on materials processed in conventional processes.Using microstereolithgraphy there is wider choice of materials such as Ceramics, Polymers, metal powder etc.

Types of Microstereolithographic Process

Scanning Type

After dividing 3-D structure into planar layers, each layer/section is scanned by light (LASER) line by line. Here the entire section is not exposed to light at a time.

Dynamic Mask Type

After dividing 3-D structure into planar layers, each layer/section is exposed to light at a time. Here the mask changes its shape dynamically. So after exposing one entire layer to light, mask changes its size & next entire section is exposed to light.

Scanning Type

A laser curable photopolymer liquid is kept in a tank.An elevator which can be moved in vertical direction is used to expose new layer after exposing one layer to light.The movement of laser beam in one direction can be achieved by means of rotating mirror. Typically two mirrors are used so that scanning in two directions (perpendicular to each other) can be done.

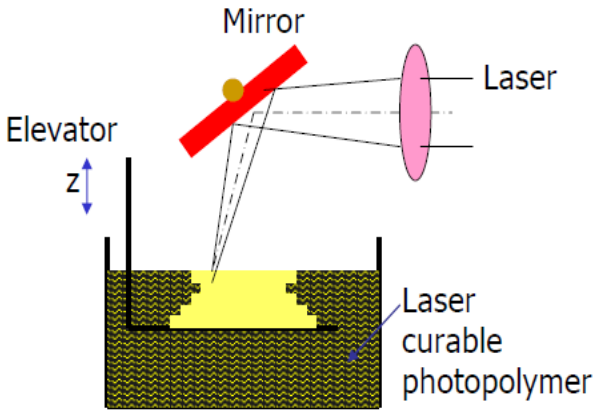


Fig: schematic diagram for scanning type

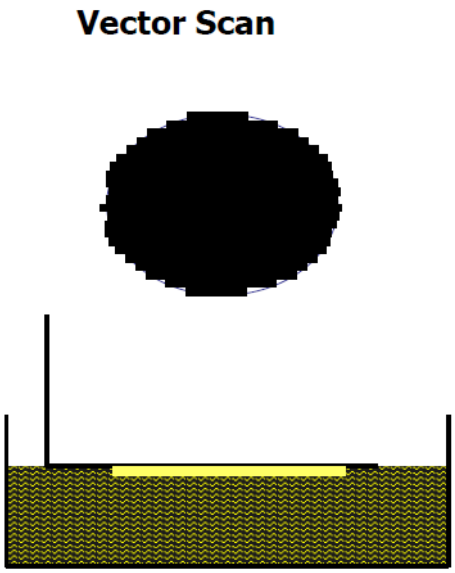


Fig: vector scan

Elevator which is initially above liquid level in tank is dipped into tank to certain depth & again brought up so that liquid of suitable thikness is on the top of it. Then it is exposed to laser. As scanning is line by line (Vector scan), the actual section will be slightly different from desired one. Generally accuracy is 5-10% which can be tolerated in case of large sections but in case of submicron components it can not be tolerated.This is the limitation of this type of process. This is used to build components having dimensions above 30 micron size. Once the section is built, the elevator is dipped again so that surface tension effects will gone & once again it is brought up so that suitable thickness of liquid is on top.Then same procedure is repeated for next section which will be built on previous section.

Dynamic Mask Type

In dynamic type, the mask changes its shape dynamically in which required area is kept bright & remaining is kept dark. Inherent disadvantage of this process is that higher power of LASER will damage mask. In this process entire section is exposed to light at a time. The remaining set-up is just like the one used in case of scaning type. There is reasonable accuracy with this type of process than the scanning type.

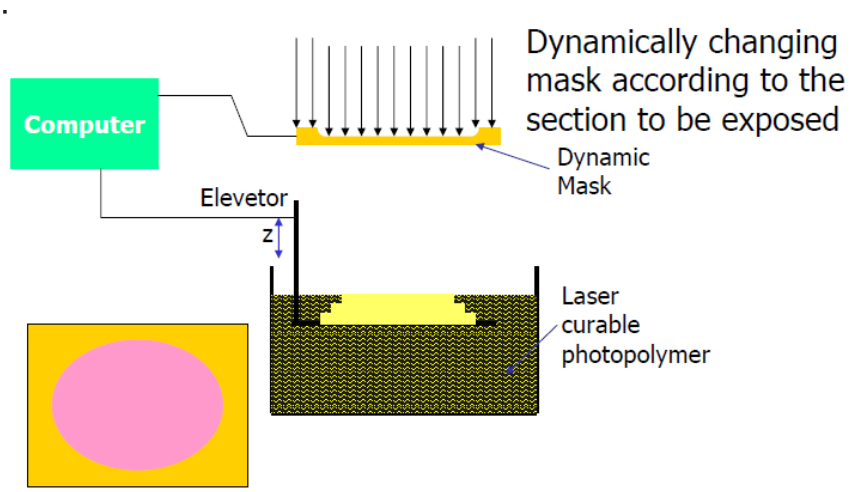


Fig: schematic diagram for dynamic mask type

Limitations

- Smooth 3D surfaces are difficult to produce with this as stepping effects will always be present.
- Mass production of several components is another challenge.
- Extremely small features are difficult to produce.

Microsystem packaging

Most MEMS and microsystem packaging has been carried out on the basis of specific applications by the industry. A major challenge to MEMS and microsystem packaging is that the core elements of these products, such as microsensors and actuators, usually involve delicate complex three-dimensional geometry made of layers of dissimilar materials. They are often

required to interface with environmentally unfriendly working media such as hot pressurized fluids or toxic chemicals. Interface is thus a major concern in microsystems packaging.

General considerations in packaging design

Proper packaging of MEMS and microsystems products is a critical factor in the overall product development cycle. Following are the principal design requirements that engineers should consider :

1. The required costs in manufacturing, assembly, and packaging of the components
2. The expected environmental effects, such as temperature, humidity, and chemical toxicity that the product is designed
3. Adequate overcapacity in the packaging design for mishandling and accidents
4. Proper choice of materials for the reliability of the package
5. Achieving minimum electrical feed-through and bonds in order to minimize the probability of wire breakage and malfunctioning

Levels of microsystem packaging

Microsystem packaging can be categorized in three levels:

Level 1: die level

Level 2: device level

Level 3: system level

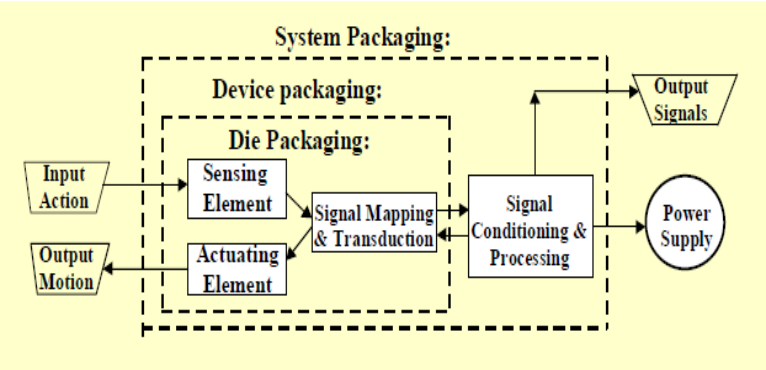


Fig: Three levels of microsystem packaging

Die-level packaging

Die-level packaging involves the assembly and protection of many delicate components in microdevices. It often involves wire bonding. The primary objectives are:

- To protect the die or other core elements from plastic deformation and cracking,
- To protect the active circuitry for signal transduction of the system,
- To provide necessary mechanical isolation of these elements, and
- To ensure the system functioning at both normal operating and over-load conditions.

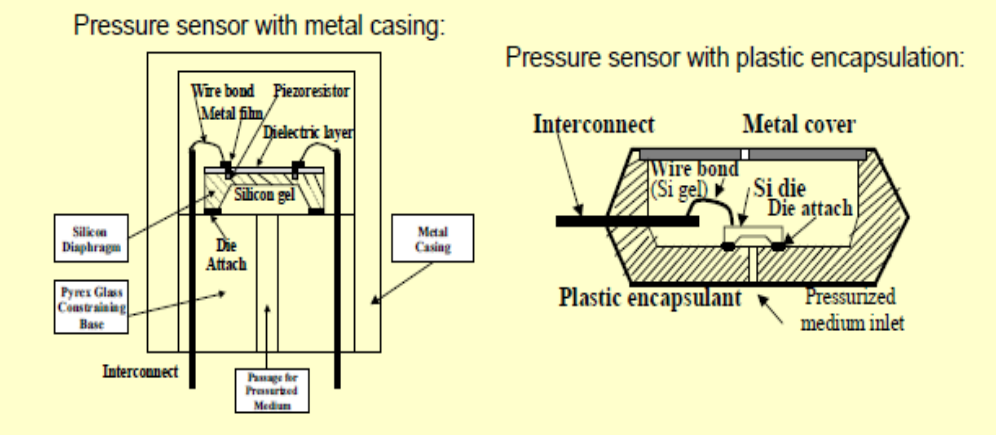


Fig: Die level packaging of micro pressure sensor

Device – Level packaging

Device packaging requires the inclusion of proper signal conditioning and processing, which in most cases involves electric bridges and signal conditioning circuitry for sensors and actuators. Proper regulation of input electric power is always necessary. A major challenge to design engineers at this level of packaging is the problems associated with interface. There are two aspects to interface problems:

1. The interfaces of delicate dice and core elements with other parts of the packaged product at radically different sizes

2. The interfaces of these delicate elements with the environmental factors such as temperature, pressure, and toxicity of the working and the contacting media.

System-Level Packaging

System-level packaging involves the packaging of primary signal circuitry with the die or core element unit. System packaging requires proper mechanical and thermal isolation as well as electromagnetic shielding of the circuitry. Metal housings usually give excellent protection from mechanical and electromagnetic influences. The interface issue at this level of packaging is primarily the fitting of components of radically different sizes. Assembly tolerance is a more serious problem at this level of packaging than at the device level.

Previous year questions

1. Explain why isotropic etching is hardly used in micro manufacturing
2. Differentiate between isotropic and anisotropic wet etching
3. Explain LIGA process with neat diagram
4. Differentiate between bulk and surface micromachining
5. What are the essential technologies that are necessary for packaging microsystem product? Explain each of them with figures
6. Explain the features of bulk micromachining
7. Explain microsystem design considerations
8. Write notes on three levels of microsystem packaging
9. Explain various steps and materials involved in surface micromachining
10. Describe chemical etching and plasma etching
11. State the need for packaging
12. Discuss the objectives of microsystem packaging. Describe the three levels of packaging
13. Describe the steps involved in the fabrication of cantilever using surface micromaching technique
14. Expalin the properties of various chemicals used for anisotropic wet etching

15. Illustarte DRIE process with neat diagram

Last year questions

1. State two advantages of LIGA process over other micro manufacturing techniques. Explain with block diagram the steps in LIGA process. State atleast one commonly used chemical in each step
2. Describe the role of sacrifical layers in surface micromachining with figures. Give two examples of two sacrificial materials used in microsystem fabrication
3. State the challenges involved in designing packages for microsystems
4. Explain with figures the steps in surface micromachining. Discuss the various fabrication challenges associated with surface micromachining
5. Give five relevant points of comparison between bulk and surface micromachining
6. Explain with figure DRIE and Plasma etching
7. Explain the levels of microsysyem packaging