

## Module - 4

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## I SEQUENTIAL CIRCUIT

In combinational circuit the output at any instant of time are entirely dependent upon the inputs present at that time. Sequential circuit consists of a combinational circuit to which memory elements are connected to form a feedback path. Memory elements are devices capable of storing binary information within them.

### State

Binary information stored in the memory elements at any given time defines the state of the sequential circuit.

The sequential circuit receives binary information from external inputs. These inputs, together with present state of memory elements, determine the binary value at the output terminals.

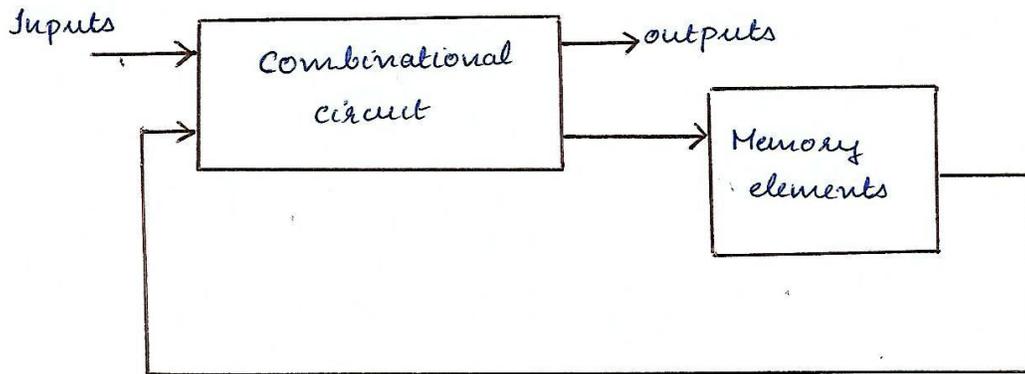


fig. Block diagram of a sequential circuit

Block diagram demonstrates that the external output in a sequential circuit are a function not only of external inputs but of the present of the memory elements. Sequential circuit is

specified by a time sequence of inputs, outputs and internal states.

### Types of Sequential Circuits

Sequential circuits are classified depending on the timing of their signals.

- a) Synchronous Sequential Circuit
- b) Asynchronous Sequential Circuit

#### a) Synchronous Sequential Circuit

Output changes at discrete interval of time. It is a circuit based on an equal state time or a state time defined by external means such as clock.

eg. Flip flops, Synchronous counter

#### b) Asynchronous Sequential Circuit

Output can be changed at any instant of time by changing the input. It is a circuit whose state time depends solely upon the internal logic circuit delays

eg. Asynchronous Counter

Synchronization is achieved by a timing device called a master-clock generator which generates a periodic train of clock pulses.

### Clocked Sequential Circuits

Synchronous sequential circuits that use clock pulses in the inputs of memory elements are called clocked sequential circuits.

#### Flip-flops

Memory elements used in clocked sequential circuits are called flip-flops. Flip flops are capable of storing one bit of information. A flip flop has one for the normal value and one for the complement

value of the bit stored in it.

## II LATCHES

Latch is a type of temporary storage device that has two stable states. Latches are similar to flip-flops because they are bistable devices that can reside in either of two states using a feedback arrangement; in which the outputs are connected back to the opposite inputs.

The main difference between latches and flip-flop is the method used for changing their state.

Three types of latch

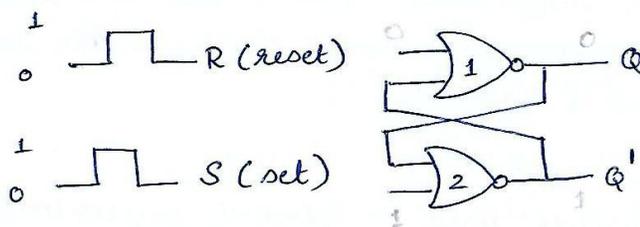
- ✓ S-R (SET-RESET) latch
- ✓ Gated S-R latch
- ✓ Gated D latch

## III FLIP FLOPS

A flip flop circuit can maintain a binary state indefinitely until directed by an input signal to switch states.

### c) Basic flip flop circuit

A flip flop circuit can be constructed from two NAND gates or two NOR gates.

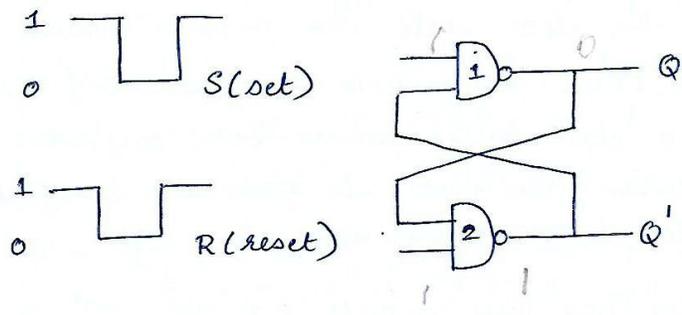


S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

a) logic diagram

b) Truth table

fig. Basic flip-flop circuit with NOR gates



a) Logic diagram

S	R	Q	Q'
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

b) Truth table

fig. Basic flip-flop circuit with NAND gates.

The cross-coupled connection from the output of one gate to the input of the other gate constitutes a feedback path. Each flip-flop has two outputs Q and Q' and two inputs set and reset. This type of flip flop is called direct coupled RS flip flop or SR latch.

When a 1 is applied to both the set and the reset inputs, both Q and Q' output go to 0. This condition violates the fact that outputs Q & Q' are the complements of each other.

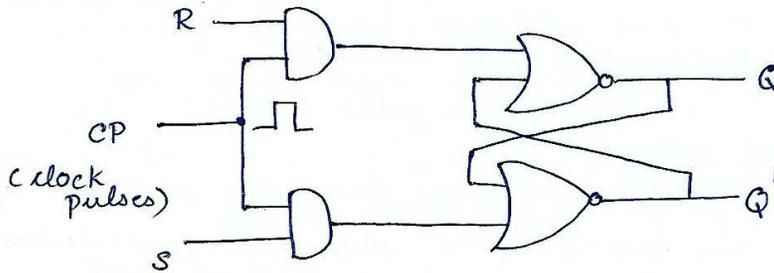
A flip flop has two useful states. When Q=1 and Q'=0, it is in the set state. When Q=0 and Q'=1 it is in the clear state (0-state).

ii) Clocked RS Flip-flop

The clocked RS flip flop consists of a basic NOR flip flop and two AND gates. The output of the two AND gates remain at 0 as long as the clock pulse is 0, regardless of the S and R input values. When the clock pulse goes to 1, information from the S and R inputs is allowed to reach the basic flip-flop. The set state is reached with S=1, R=0 and CP=1.

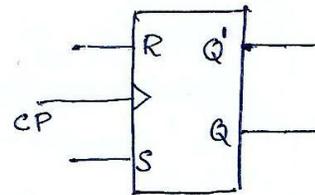
To change to the clear state, the inputs must be  $S=0, R=1$  and  $CP=1$ . With both  $S=1$  and  $R=1$  the occurrence of a clock pulse causes both outputs to go to 0. When the pulse is removed the state of the flip flop is indeterminate.

RS flip flop has three inputs  $S, R, CP$ .



a) Logic Diagram

Q	S	R	$Q(t+1)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	indeterminate



b) Graphic symbol

c) Characteristic table

Q \ SR	$S'R'$ 00	$S'R$ 01	$SR$ 11	$SR'$ 10
$Q'$ 0			X	1
$Q$ 1	1		X	1

$$Q(t+1) = \overline{QR'} + S$$

$SR=0$

d) Characteristic equation

In graphic symbol CP input is not written within the box because it is recognized using small triangle. The triangle is a symbol for a dynamic indicator and denotes the fact that the flip flop responds to an input clock transition from a low-level (binary 0) to a high level (binary 1) signal.

The outputs of the flip flop are marked with  $Q$  and  $Q'$ . The characteristic table summarizes the operation of the flip-flop in a tabular form.  $Q$  is the binary state of the flip flop (referred as present state),  $S$  &  $R$  are inputs,  $Q(t+1)$  is the state of the flip-flop after the occurrence of a clock pulse (next state)

Characteristic equation of the flip flop is derived in the map. Equation specifies the value of the next state as a function of the present state and the inputs. Two indeterminate state are marked by X's in the map, as they result in either 1 or 0

### iii) D Flip flop

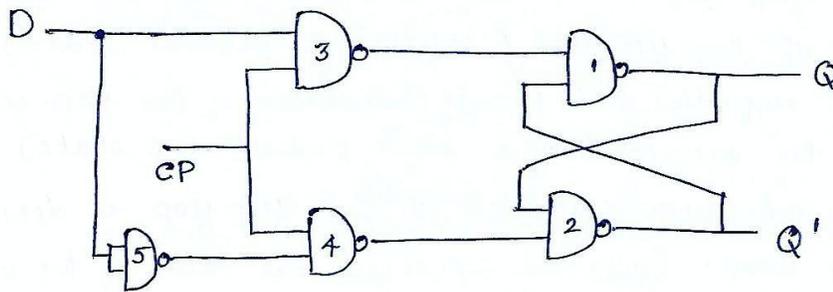
The D flip flop is a modification of the clocked RS flip flop. NAND gates 1 and 2 form a basic flip flop and gates 3 and 4 modify it into a clocked RS flip flop. The D input goes directly to the S input, and its complement through gate 5, is applied to the R input.

When clock pulse input is 0, gate 3 & 4 have a 1 in their output regardless of the value of the other inputs. Therefore the two inputs of a basic NAND flip flop remain initially at 1.

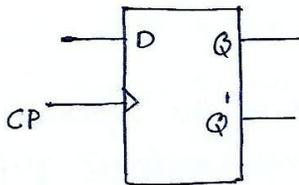
If D is 1, the output of gate 3 goes to 0, switching the flip flop to the set state. If it is 0, the output of

gate 4 goes to 0, switching the flip flop to the clear state.

The D flip flop got its name 'D' from its ability to transfer "data" into a flip-flop. D flip flop is basically an RS-flip flop with an inverter in the R input. Added inverter reduces the number of inputs from two to one. This flip flop is also called gated D-latch



a) Logic diagram with NAND gates



b) Graphic symbol

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

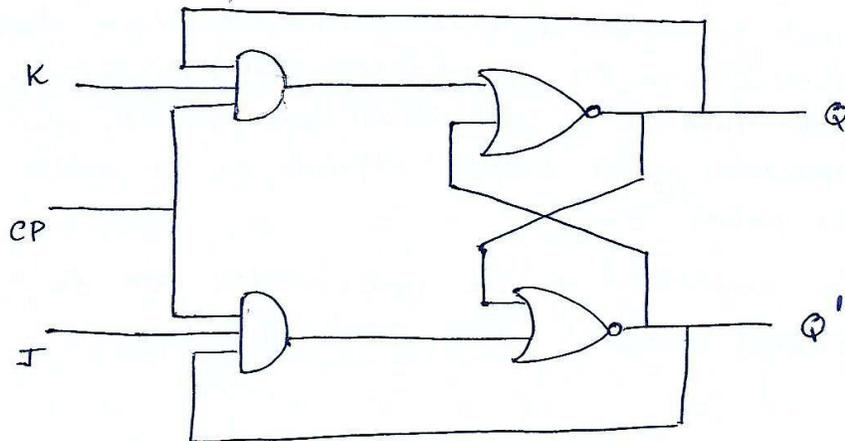
c) Characteristic table

		D	
		D'	D
Q'	0	0	1
	1	0	1

$Q(t+1) = D$  d) Characteristic equation

### iv) JK flip flop

JK flip-flop is a refinement of the RS flip flop, The indeterminate state of RS type is defined in the JK type. Inputs J and K behave like inputs S & R to set and clear the flip flop. In a JK flip flop, the letter J is for set and the letter K is for clear. When inputs are applied to both J & K simultaneously the flip-flop switches to its complement state if  $Q = 1$ , it switches to  $Q = 0$  and vice versa.



a) Logic diagram

Output  $Q$  is ANDed with  $K$  and  $CP$  inputs, so that the flip flop is cleared during a clock-pulse only if  $Q$  was previously 1. Similarly output  $Q'$  is ANDed with  $J$  and  $CP$  inputs so that the flip flop is set with a clock pulse only if  $Q'$  was previously 1.

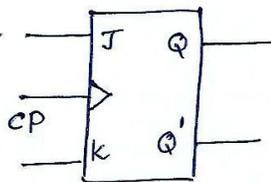
JK flip flop behaves like an RS flip flop, except when both  $J$  &  $K$  are equal to 1. When both  $J$  and  $K$  are 1, the clock pulse is transmitted through one AND gate only - the one whose input is connected to the flip flop output which is presently equal to 1.

If  $Q = 1$ , the output of the upper AND gate becomes 1 upon application of a clock pulse, and the flip flop is cleared.

If  $Q' = 1$  the output of the lower AND gate becomes a 1 and the flip flop is set. In both case, the output state of the flip flop is complemented.

Because of the feed back connection in the JK flip flop, a CP signal which remains a 1 (with  $J = K = 1$ ) after the outputs have been complemented once will cause repeated and continuous transitions of the outputs. To avoid this undesirable operation, the clock pulses must have a time duration which is shorter than the propagation delay through the flip flop. This is a restrictive requirement, since the operation of the circuit depends on the width of the pulses.

The restriction on the pulse width can be eliminated with a master-slave flip flop.



b) Graphic symbol

Q	J	K	$Q(t+1)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

c) characteristic table

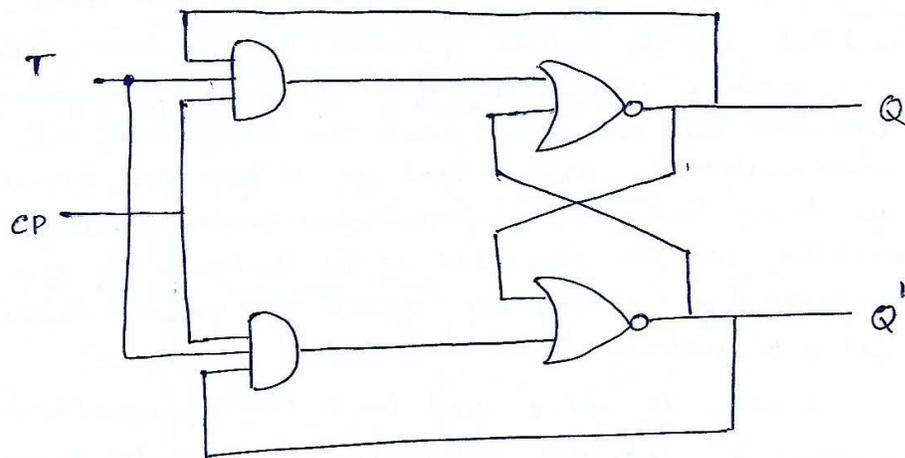
JK	$J'K'$	$J'K$	JK	$JK'$
00	01	11	10	
$Q'$ 0	0	0	1	1
Q 1	1	0	0	1

$$Q(t+1) = QK' + Q'J$$

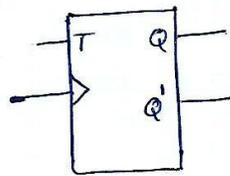
## v) T- Flip flop

The T flip flop is a single-input version of the JK flip flop. The T flip flop is obtained from a JK type if both inputs are tied together. The T flip flop got its name 'T' from the ability of the flip flop to "toggle" or change state.

Regardless of the present state of the flip flop, it assumes the complement state when the clock pulse occur while input T is logic-1.



a) Logic Diagram



b) Graphic symbol

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

c) Characteristic table

	T	T'	T
Q			
Q'			1
Q	1		

$$Q(t+1) = QT' + Q'T$$

d) Characteristic equation

#### IV TRIGGERING OF FLIP FLOPS

The state of a flip-flop is switched by a momentary change in the input signal. This momentary change is called a trigger and the transition it causes is said to trigger the flip flop. Asynchronous flip flops, such as basic circuits requires an input trigger, clocked flip flops are triggered by pulses.

A pulse starts from an initial value of 0 goes momentarily to 1 and after a short time, returns to its initial 0 value. The feedback path can produce instability if the outputs of memory elements are changing while the outputs of the combinational circuit that go to flip flop inputs are being sampled by the clock pulse. Timing problem can be prevented if the outputs of flip flop do not start changing until the pulse input has returned to 0.

A way to solve feed back timing problem is to make the flip flop sensitive to the pulse transition rather than the pulse duration.

A clock pulse may be either positive or negative. A positive clock source remains at 0 during the interval between pulses and goes to 1 during the occurrence of a pulse.

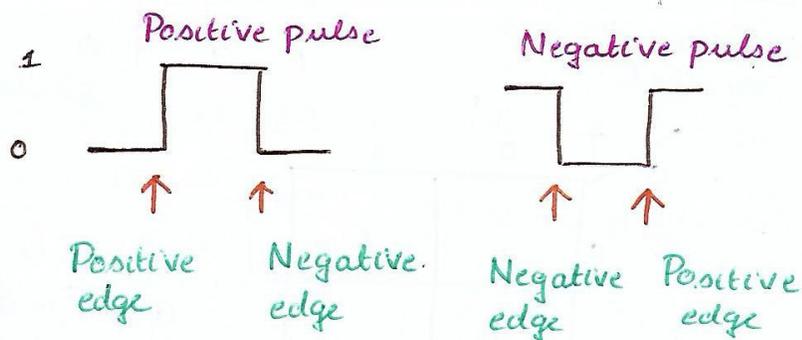


fig. Definition of clock pulse transition

The pulse goes through two signal transitions from 0 to 1 and the return from 1 to 0. The positive transition is defined as the positive edge and the negative transition as the negative edge. Clocked flip flops are triggered during the positive edge of the pulse and the state transition starts as soon as the pulse reaches the logic 1 level.

### V MASTER - SLAVE FLIP FLOP

A master slave flip-flop is constructed from two separate flip flops. One circuit serves as a master and the other as a slave, and the overall circuit is referred to as a master-slave flip flop.

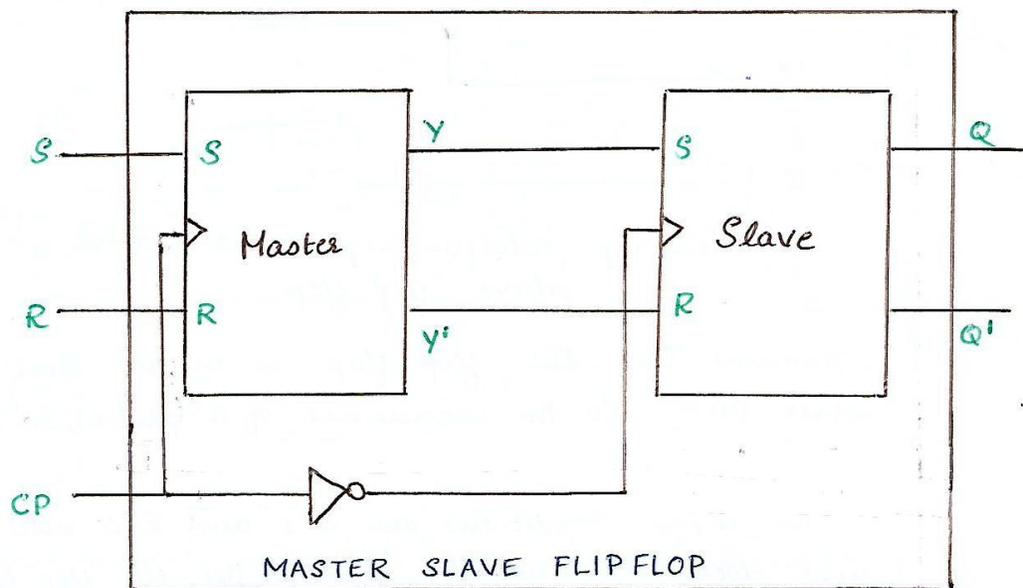


fig logic diagram of master-slave flip flop.

Consists of a master flip flop, a slave flip flop and an inverter. When clock pulse is 0, the output of the inverter is 1. When the clock input of the slave is 1, the flip flop is enabled and output Q is equal to Y, & Q' is equal to Y'. The master flip flop is disabled because CP=0.

When the pulse becomes 1, the information at the external R and S inputs is transmitted to the master flip-flop. The slave flip flop is isolated as long as the pulse is at its 1 level, because the output of the inverter is 0. When the pulse returns to 0, the master flip flop is isolated, which prevents the external inputs from affecting it.

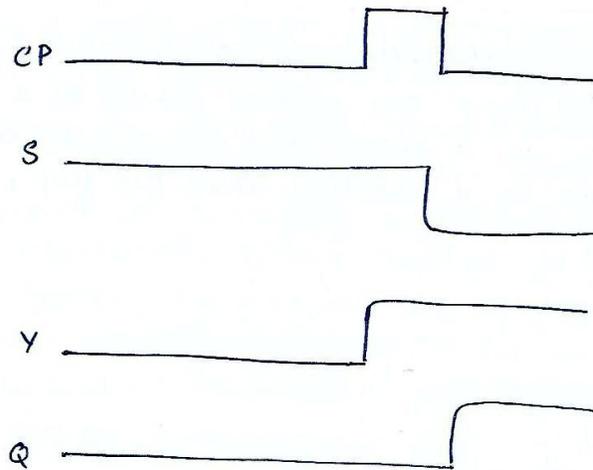


fig. Timing relationships in a master slave flip flop

Assume that the flip flop is in the clear state prior to the occurrence of a pulse, so that  $Y=0$  and  $Q=0$

The input conditions are  $S=1$  and  $R=0$  and the next clock pulse should change the flip flop to the set state with  $Q=1$ . During the pulse transition from 0 to 1 the master flip-flop is set and changes Y to 1. The slave flip flop is not affected because its CP input is 0. Since master flip flop is an internal circuit its change of state is not noticeable in the output  $Q$  &  $Q'$

When pulse returns to 0, the information from the master is allowed to pass through to the slave

making the external output  $Q=1$ . External  $S$  input can be changed at the same time when the pulse goes through its negative edge transition, because once the CP reaches 0, the master is disabled and its R and S inputs have no influence until the next clock pulse.

Master slave combination can be constructed for any type of flip flop by adding a clocked R-S flip flop with an inverted clock to form the slave.

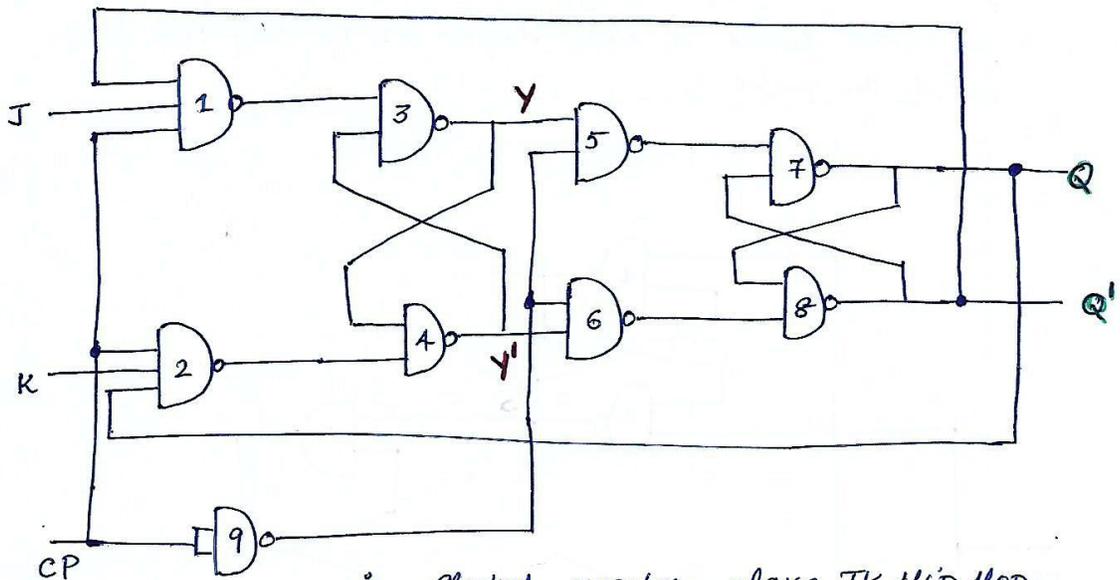


fig. Clocked master-slave JK flip flop

It consists of 2 flip flops. Gates 1 through 4 form the master flip flop and gates 5 through 8 form the slave flip flop.

Information present at J and K inputs is transmitted to the master flip-flop on the positive edge of a clock pulse and held there until the negative edge of the clock pulse occurs, after which it is allowed to pass through to the slave flip-flop.

## VI EDGE TRIGGERED FLIP FLOP

Edge triggered flip flop is a type of flip flop that synchronizes the state changes during a clock pulse transition. Output transitions occur at a specific level of the clock pulse. When the pulse input level exceeds this threshold level, the inputs are locked out and the flip-flop is unresponsive to further changes in inputs until the clock pulse returns to 0 and another pulse occurs.

Some edge-triggered flip flops cause a transition on the positive edge of the pulse and others cause a transition on the negative edge of the pulse.

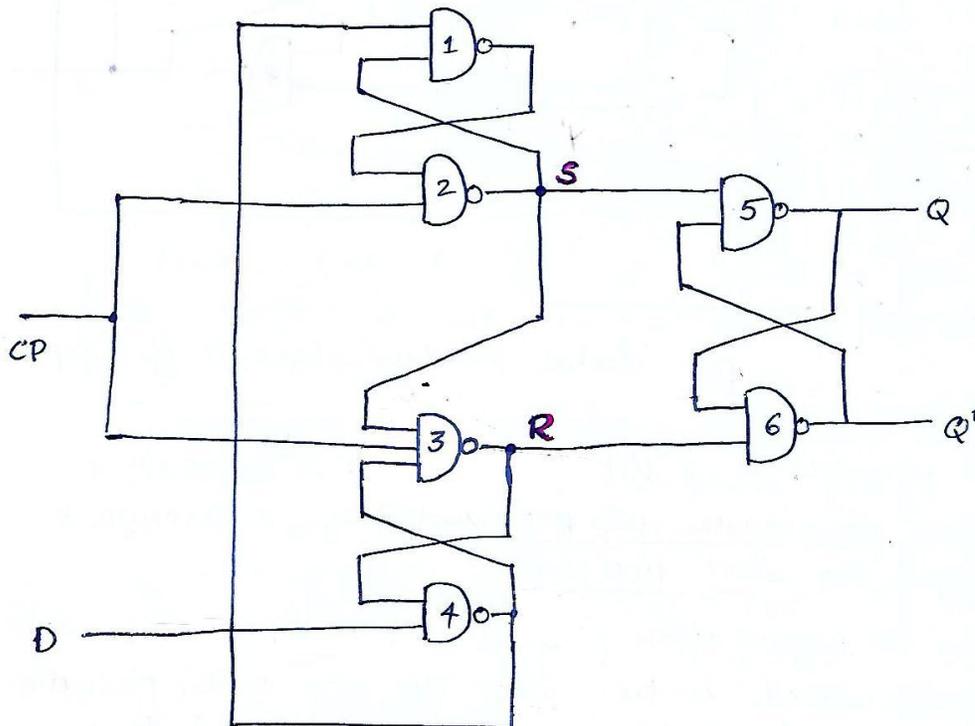


fig. D type positive-edge triggered flip flop

The logic diagram of a D-type positive edge triggered flip flop consist of three basic flip flop. NAND gates 1 and 2 make up one basic flip flop and gates 3 and 4 another. The third basic flip flop, gates 5 and 6 provide the output to the circuit.

Inputs S and R of the third basic flip flop must be maintained at logic 1 for the outputs to remain in their steady state values. When  $S=0$  and  $R=1$ , the output goes to the set state with  $Q=1$ . When  $S=1$  and  $R=0$  the output goes to the clear state with  $Q=0$ . Inputs S and R are determined from the states of the other two basic flip flops. These two basic flip flop respond to the external inputs D (data) and CP (clock pulse).

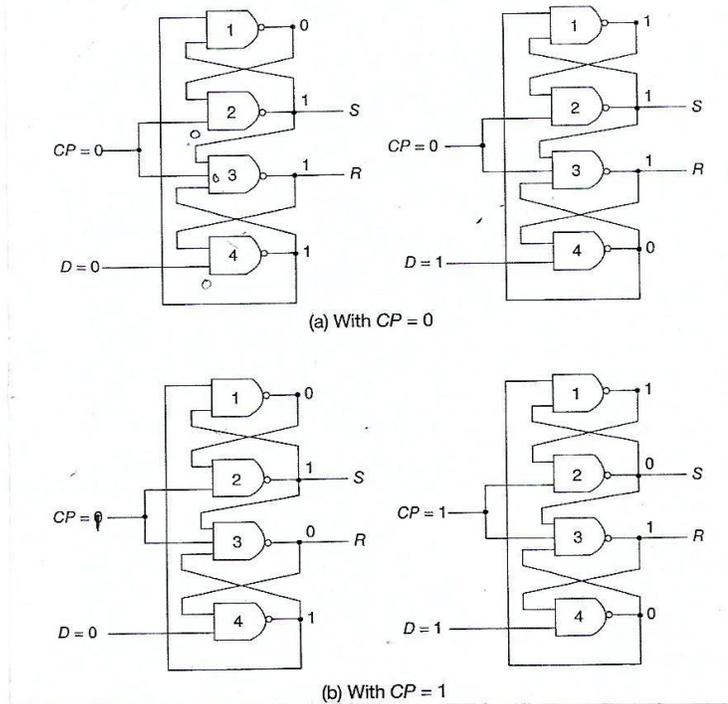


fig. Operation of the D-type edge triggered flip flop

Figure shows the binary values at the outputs of the four gates when  $CP=0$ . Input  $D$  may be 0 or 1. In either case, a  $CP$  of 0 causes the outputs of gates 2 and 3 to go to 1, thus making  $S=R=1$ , which is a condition for a steady state output. When  $D=0$ , gate 4 has a 1 output, causes the output of gate 1 to go to 0.

When  $D=1$ , gate 4 goes to 0, which causes the output of gate 1 to go to 1.  $CP=0$ , disables any changes at the outputs of the flip flop, no matter what the value of  $D$  happens.

### Set up time

There is a definite time, called the setup time in which the  $D$  input must be maintained at a constant value prior to the application of the pulse.

### Hold time

There is a definition time, called the hold time, that the  $D$  input must not change after the application of the positive-going transition of the pulse.

When the input clock pulse makes a positive going transition the value of  $D$  is transferred to  $Q$ . Changes in  $D$  when  $CP$  is maintained at a steady 1 value do not affect  $Q$ .

VII

### RACE AROUND CONDITION

In JK flip-flop, the output is feedback to the input and therefore change in the output results change in the input.  $J=K=1$  and  $Q=0$ . When a clock pulse with a width ' $t_p$ ' is applied, the

output will change from 0 to 1 after the time interval  $\Delta t$

where  $\Delta t$  = propagation delay of two level NAND gates

$t_p$  = pulse width

After  $\Delta t$ , we have  $J=K=1$  and  $Q=1$  and after another  $\Delta t$ , output  $Q$  will become 0. Hence, the output will oscillate back and forth between 0 and 1 in the duration  $t_p$  of the clock pulse width. So at the end of clock pulse, the value of  $Q$  is ambiguous. This situation is known as a 'race-around condition'.

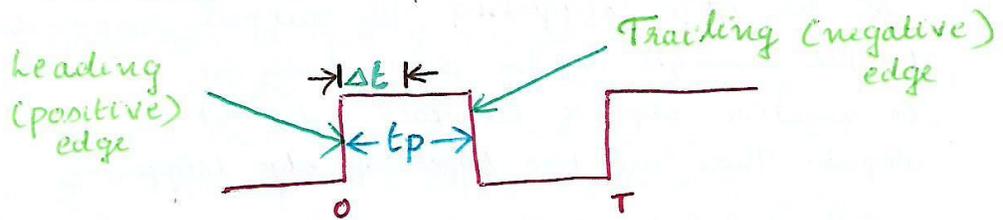


fig. 7 clock pulse

The race around condition can be avoided when  $t_p < \Delta t$ . This can be obtained in two ways

- a) If  $t_p$  is reduced
- b) If  $\Delta t$  is increased

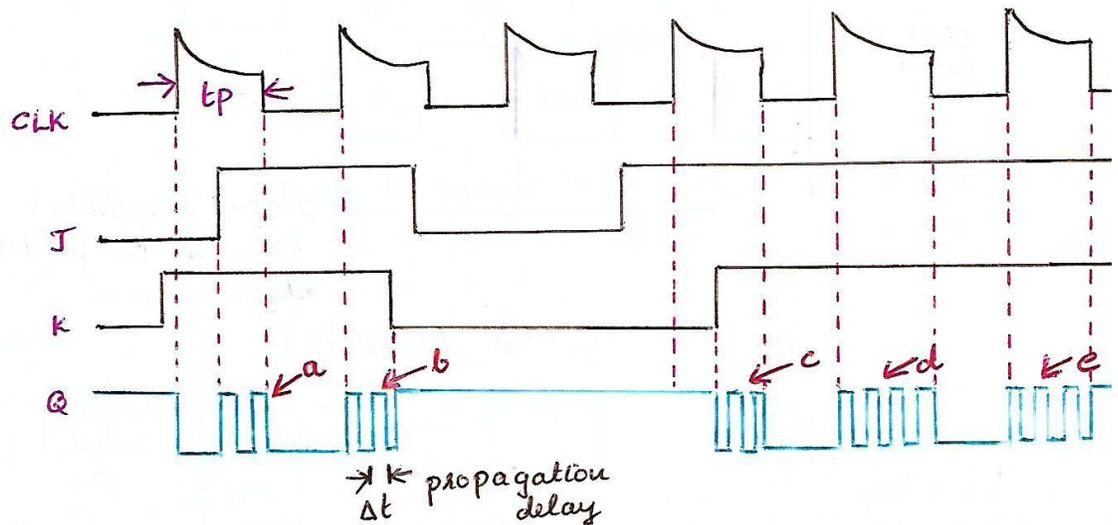


fig Input and output waveforms for clocked JK flip flop

The race around condition can be avoided if

- \* The propagation delay caused by NAND gates is greater than the clock interval. But practically that is not possible since the propagation delay in integrated chip is very small.
- \* Master slave flip flop is used instead of JK flip flop.

IX

### EDGE TRIGGERING & LEVEL TRIGGERING

In the edge triggering, the output responds to the changes in the input only at the positive or negative edge of the clock pulse at the clock input. There are two types of edge triggering

- Positive edge triggering
- Negative edge triggering

Positive edge triggering: The output responds to the changes in the input only at the positive edge of the clock pulse at the clock input

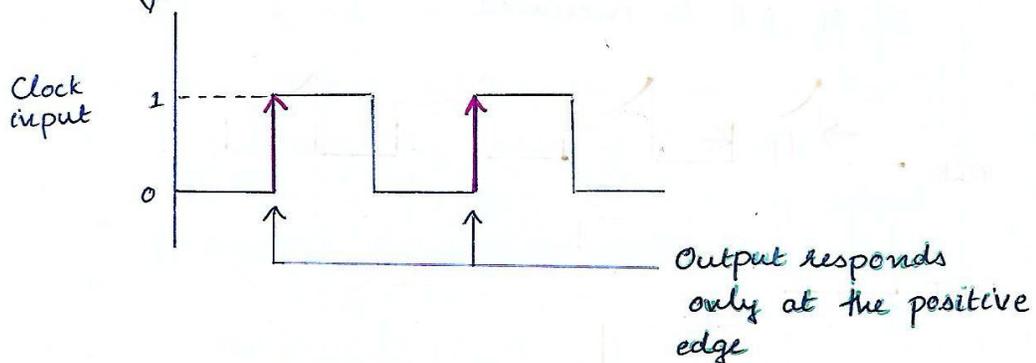
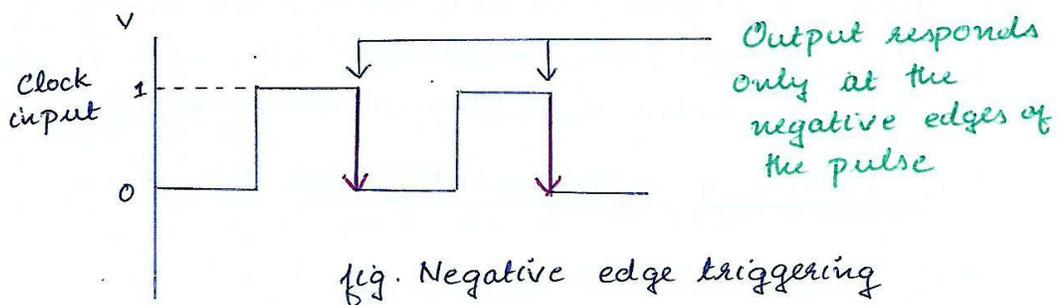


fig Positive edge triggering

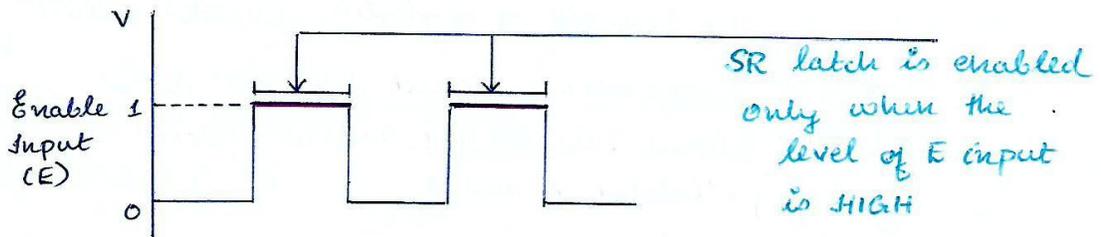
Negative Edge triggering: The output responds to the changes in the input only at the negative edge of the clock pulse at the clock input.



### Level triggering

In level triggering the output state is allowed to change according to inputs when active level is maintained at the enable input. There are two types of level triggered latches:

Positive level triggered: The output of latch responds to the input changes only when its enable input is 1 (high)



Negative level triggered: The output of latch responds to the input changes only when its enable input is 0 (low)

